IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC., Plaintiff, v. FREESCALE SEMICONDUCTOR, INC., Defendant.	)	C.A. No. 06-788 (JJF)

APPENDIX TO FREESCALE'S OPENING CLAIM CONSTRUCTION BRIEF
VOLUME IV; EXHIBITS RELATING TO THE CHAN PATENTS
CHAN FILE HISTORIES AND DICTIONARIES

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Dated: November 6, 2007

TABLE OF EXHIBITS

EXHIBIT 8

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/546,071	06/27/90	CHAN A	M-1018-US

EXAMINER
POPEK, J

DAVID H. CARROLL
SKJERVEN, MORRILL, MAC PHERSON,
FRANKLIN AND FRIEL
25 METRO DRIVE, STE. 700
SAN JOSE, CA 95110

ART UNIT	PAPER NUMBER
233	5

DATE MAILED: 04/08/91

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ~~_____ days~~ from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 1 to 3 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1 to 3 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev.9-89)

Claims 1 to 3 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 2 to 4, it is not clear how the ports are coupled to the random access memory. Lines 8 to 10 are confusing. Does the output register resupply the received data back to the system port? In claim 2, the input register appears to be performing the same function as the output register as recited in lines 9 and 10 of claim 1. Does the input register provide the received data from the memory back to the system port? How is the input register coupled with the output register? In claim 3, line 4, "data" is not clear. Is applicant referring to the received data from the memory? On line 5, "data" is not clear. How is the data related to the received data of line 8 in claim 1?

The Abstract of the Disclosure is objected to because it is not limited to a single paragraph. Correction is required. See M.P.E.P. § 608.01(b).

Applicant is reminded of the proper language and format of an Abstract of the Disclosure.

> The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 250 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such

as "means" and "said", should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," *etc.*

J. Popek/mb
April 05, 1991
(703)308-3124

JOSEPH A. POPEK
PRIMARY EXAMINER
ART UNIT 233

EXHIBIT 9

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/678,912	04/01/91	CHAN	~~A~~ M-1018-1P-US

EXAMINER
GOSSAGE, G

E3M1/0909

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ART UNIT	PAPER NUMBER
2312	6

DATE MAILED: 09/09/93

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on 10-21-91 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ~~____ days~~ from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☑ Notice re Patent Drawing, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449. (2)
4. ☐ Notice of Informal Patent Application, Form PTO-152.
5. ☑ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 1-18 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 1-18 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☑ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 9-89)

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 C.F.R. § 1.67(a) identifying this application by its Serial Number and filing date is required. See M.P.E.P. §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not state that the person making the oath or declaration has reviewed and understands the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration.

The phrase "including the claims" must be included. Any amendments made before the signing of the new oath or declaration should also be acknowledged.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. A suggestion for a new title is not readily apparent to the Examiner.

3. The Abstract of the Disclosure is objected to because it should generally be limited to a single paragraph. In lines 4-5 and 8, "The (the)" should be -- A(a) -- to avoid possible antecedent problems. [Note that abstract line numbers are given, not page line numbers.] In lines 19 and 21, -- random access -- should be inserted before "memory" for clarity.

It also appears the second paragraph (lines 16-25) should be moved after "transfers." in line 3.

Additionally, in lines 3-4, '"demand word first" wrapped around quad fetch order' is not fully understood.

Correction is required. See M.P.E.P. § 608.01(b).

4. The numerous sheets/figures of drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the drawings.

Upon a quick review of the drawings, the following items were noted and the drawings are objected to for the following reasons:

In Figures 6 and 7, the dashed boxes 3167 and 4167 should be descriptively labelled. The box "245" should also be descriptively labelled.

In Figures 8A, 8B and 8C, (at least) a representative one of each of the different circuit "boxes" should be labelled for clarity. The darkened triangular symbol is also not sufficiently clear. The boxes I-IV are confusing and should be descriptively labelled.

In Figure 12B, the "dangling" (not connected to the other circuit elements) cycle/control unit should be separately labelled (-- Fig. 12c --) or output signals shown which correspond to inputs to other circuits. It is also not clear to what the labels "SYSTEM (HOST) PORT" refer.

In Figure 13, the label "SYSTEM" is not clear (-- SYSTEM PORT --?). The box 70 should be descriptively labelled. One of

the 4 boxes labelled "MS82C443" should be descriptively labelled.

In Figure 14, the boxes/circuits should be descriptively labelled.

In Figure 15, "MUPREG" should be -- MEM. UPDATE REG. -- for clarity.

In Figure 32, "with 4167" is not sufficiently clear. A descriptive label should be added after "4167."

In Figure 53, the labels "tmi/thi", "thi1xI" and "thi1xU" are not sufficiently clear. The label "Bram" is also not clear (-- Burst RAM -- ?). The labels "ttmiss" and "tlmiss" are also unclear, as are the labels (code?) within the steps. The newly added labels ("assert brdy # ..." and "cache : assert ....") are not understood (to what do those labels refer or correspond?). Figures 54-56 are analogously unclear.

Similarly, in Figures 57-58, the labels "ctiout", "ctblout", etc. are not adequately clear.

Note that these are merely exemplary. Applicant should carefully and completely review all of the figures to ensure that all possible errors are located and corrected. The timing diagrams (Figures 16-31 e.g.), not specifically discussed above by the Examiner, should be carefully reviewed and corrected where appropriate.

Applicant is required to submit a proposed drawing correction in response to this Office action. However,

correction of the noted defect can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02 (r) and (v).

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following items are specifically noted and the specification objected to for the following reasons:

On page 1, line 6, the status of the related copending application should be updated.

On page 2, line 21, and throughout the specification (and drawings), the notation "#" is confusing as this notation/labelling does not appear to have a well known or commonly accepted meaning in the art (active low? complement of the signal?). An explanatory sentence should be inserted after the first use of the symbol for clarity.

On page 7, line 34 and throughout the specification (page 15, line 8; page 16, line 12 and page 43, line 1, by way of example), there is no "Figure 8." The term should be replaced with -- Figures 8A, 8B and 8C -- (or simply -- Figure 8A --, -- Figure 8B --, etc.) where appropriate.

On page 19, (approximately) lines 34-37, "associates with" is awkward. It appears -- is associated with -- is clearer.

On page 37, line 17, "controller" should be -- Controller --

.

Again, these are merely exemplary. Applicant's cooperation is again requested in locating and correcting all possible errors to place the specification in proper idiomatic and grammatical form.

6. Claims 1-18 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, and therefore its dependent claims, "said data" (line 9) has an unclear antecedent (see lines 6 and 8). Note the clearer language of claim 4. Also, in lines 6 and 8, "said memory" may have an unclear antecedent. It appears -- random access -- should be inserted before "memory" in lines 6 and 8 for clarity. Also, in line 1, "memory cache" appears to read more clearly as -- cache memory --.

In claim 2, the distinction between the "input latch ... for ... writing data" of claim 1 and the "input register ... for furnishing data" (claim 2) is not sufficiently clear. Note the clearer language of claim 3, lines 1-3, for example. Also compare claim 2, lines 2-3 and claim 4, lines 5-7 (the distinction between "furnishing" and "writing" is not entirely clear).

Also in claim 4, line 1, it appears "memory cache" should be -- cache memory --. [The dependent claims should be similarly amended.] The distinction between the input register "furnishing data" (claim 2) and "writing" data (claim 4) is not entirely clear. In line 14, "when" appears to read more clearly as -- that --.

In claim 5, lines 4 and 7, "addressing" appears to read more clearly as -- address --. Also, the wording "an address(ing) signal (singular) corresponding to said ... data (plural)" is confusing. Should "an address(ing) signal" be changed (back) to -- address signals --?

In claim 6, -- random access -- should be inserted before "memory" to avoid antecedent problems.

In claim 10, line 3, "the" should be deleted.

In claim 12, "(increments from) an address associated with a first line of data to a subsequent line of data" is not clear. Should -- an address associated with -- be inserted after "to" in line 3?

In claim 13, lines 3-4, "of data of said data" is not clear. It is also not clear how "validating data" itself prevents the writing of data into RAM.

In claim 14, "includes" appears to read more clearly as -- stores --.

In claim 15, line 2, "RAM" should be written out (or --

(RAM) -- inserted after "memory" in claim 1, line 2).

In claim 17, it is not clear how a "memory 'has' a ... bandwidth."

In claim 18, it is unclear how the memory itself performs a read-modify-write operation.

7. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 1-18 are rejected under 35 U.S.C. § 103 as being unpatentable over applicant's admitted prior art in view of Aichelmann, Jr. et al. or Watanabe, each taken separately.

Applicant's admitted prior art discloses that a memory apparatus including a random access memory, a host port and a system port was well known in the computer storage art at the time the claimed invention was made, but does not disclose coupling an input buffer/register and an output buffer/register

to the memory in order to provide improved access and increased operating speed. Aichelmann, Jr. et al. or Watanabe, each taken separately, similarly discloses a computer memory apparatus and teaches coupling input and output buffers/registers to a dual port cache for the desirable purpose of providing improved memory acess and increased operating speed. Accordingly, it would have been readily obvious to a person of ordinary skill in the computer storage art at the time the claimed invention was made to utilize buffers/registers coupled to plural ports as taught by Aichelmann, Jr. et al. or Watanabe, each taken separately, in the well known memory of applicant's admitted prior art for the desirable purpose of providing improved memory access and increased operating speed. The use of hit, miss and writeback registers in conjunction with a cache memory was well known in the memory art at the time the claimed invention was made and as such does not patentably define the claimed invention over the prior art [redacted].

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wilhite et al, Wallach et al. ('275 and '317) and Matick et al. are cited as teaching cache memory arrangements similar to the claimed invention.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 9600.

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2312

G. Gossage/kw
September 08, 1993

EXHIBIT 10

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/678,912	04/01/91	CHAN A	M-1018-1P-US

GOSSAGE, EXAMINER

B3M1/0308

B. NOEL KIVLIN
SKJERVEN, MORRILL, MACPHERSON,
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25 METRO DRIVE, SUITE 700
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ART UNIT	PAPER NUMBER
2312	8

DATE MAILED: 03/08/94

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on 12-6-93 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ~~0~~ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 1-23 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 1-23 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☑ The proposed drawing correction, filed on 12-6-93, has been ☑ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 9-89)

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 C.F.R. § 1.67(a) identifying this application by its Serial Number and filing date is required. See M.P.E.P. §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not state that the person making the oath or declaration has reviewed and understands the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration.

Applicant's arguments filed December 6, 1993 have been considered but are not persuasive. It is well understood that the claims are a part of the application; however, 37 CFR 1.63 requires an explicit statement that the applicant has read and understood the contents of the specification, including the claims. The person signing the oath or declaration must recognize that what is being claimed is the subject matter that the person regards as his or her invention pursuant to 35 U.S.C. 112. See 1027 OG 9. Strict adherence to the language of 37 CFR 1.63 is believed necessary. This view was confirmed upon consultation with several other experienced Examiners and supervisors.

[Note that applicant's remarks on page 12 of the response filed December 6, 1993 regarding the filing of a new declaration are not entirely understood and appear to be inconsistent with the remarks on page 8 of the response. Since a new declaration

apparently was not filed, the remarks on page 12 have been disregarded.]

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

It appears "A Random Access Memory And Decoupling" should be simply --Decoupling Register-- for clarity. It is also noted that the term "Dual Ported" is not entirely understood when read in conjunction with claim 16.

3. The Abstract of the Disclosure is objected to because it does not provide a clear and concise summary of the disclosure. It appears the paragraph deleted in the response filed December 6, 1993 [original abstract, (page) lines 19-28] should be inserted after "transfers" in line 6 for clarity. The following changes are also suggested within that paragraph: In lines 21 and 26, "latch" should be --register-- (note claim 1, line 6, for example). In lines 22 and 24, --random access-- should be inserted before "memory."

Additionally, in lines 8 and 11, "from the" should be --from a--. In lines 6-7, it is not readily apparent what is meant by " "demand word first" wrapped around quad fetch order."

Applicant should address each of these issues by way of either amendment or argument. Note the Office action mailed September 9, 1993 at page 2, numbered paragraph 3.

Correction is required. See M.P.E.P. § 608.01(b).

4. The proposed drawing corrections filed on December 6, 1993 have been approved by the Examiner, subject to drafting review.

The drawings remain objected to, however, because in Figures 8A-8C, a representative one of each of the different circuit "boxes" should be descriptively labelled for clarity. Note "boxes" 109, 110, 158, 150, 128, 124, 166, 119, 129, 120, and 113 in Figure 8A; "boxes" 114A-114D, 116A-116D and 118A-118D in Figure 8B and "boxes" 122, 112 and 163 in Figure 8C by way of example. It may be necessary to place the reference numerals outside the circuit "boxes."

In Figure 53, the deletion of the labels within the different steps (302, 304, 306, 308 and 310, for example) is confusing. Descriptive labels should be (re)inserted for clarity. It also remains unclear to what the labels "assert: brdy#..." and "cache:assert..." refer. The significance of the newly added brackets is also not clear. The label "ads#" within step 300 is also not adequately clear. Figures 54-56 are analogously unclear.

In Figures 57-58, the removal of descriptive labels within the steps renders the Figures unclear and confusing. Clear and descriptive labels should be (re)inserted for clarity.

Again note that the numerous drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the drawings.

Applicant is required to submit a proposed drawing correction in response to this Office action. However, actual correction of the noted defect can be deferred until the application is allowed by the examiner.

Again note MPEP 608.02(r) and (v). [Proposed drawing corrections should be shown in red ink and submitted in a separate letter addressed to the Office draftsman.]

5. It is once again noted that the lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following objections are specifically noted: Throughout the specification (note page 15, line; page 16, line 12 and page 43, line 1, by way of example only), the notation

"Figure 8" is not adequately clear. In this regard, it is noted that while the notation adopted by applicant in the response filed December 6, 1993 (generally referring to "Figure 8") would be acceptable to the Examiner, this notation would create problems for the printer (should any patent issue based on this application) since there is no figure labelled "Figure 8" (many applications have been returned from the printer for just such "errors"). Thus, the specification must be reviewed and each reference to "Figure 8" replaced with a reference to --Figure 8A--, --Figure 8B--, --Figure 8C-- or --Figures 8A-8C-- where appropriate to avoid confusion and prevent possible delays in printing and issuance of any patent based on this application.

On page 19, (approximately) lines 34-37, "associates with" is awkward. It appears --is associated with-- is clearer. [Note that the proposed amendment filed December 6, 1993 has NOT been entered by the clerk since this portion of the specification is single spaced and entry of the amendments is difficult and may lead to printing errors. The entire passage (lines 34-37) should be deleted and replaced for clarity.]

6. Claims 1-23 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13, it remains unclear how simply "validating data" itself prevents the writing of data into RAM. Note also the previous Office action mailed September 9, 1993 at page 7, lines 19-21.

[It is also hereby expressly noted that while the difference in language regarding the operation of the registers ("furnishing (data)," "providing (data)" and "writing (data)" for example) is not as precise as the Examiner might desire, upon a consideration of the claim language in light of the specification, the claims are deemed sufficiently clear to meet the statutory standard of particularly pointing out and distinctly claiming the subject matter which applicant regards as his invention. Accordingly, the 35 U.S.C. 112, second paragraph, rejection based on this claim language (see the Office action mailed December 6, 1993 at page 6, lines 18-24 and page 7, lines 3-5, for example) is hereby withdrawn.]

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section

371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 4, 6-8 and 13-15 are rejected under 35 U.S.C. § 102(b) as being anticipated by Malinowski.

The broad claim language "reads on" the structure disclosed by the reference. Here, the write registers 30 and 32 are input registers and the read registers 40 and 42 constitute "output registers." The outputs of the read registers and MUX 44 may be broadly considered a "system" port, with the inputs to MUX 34 and the write registers serving as the "host port." See Figures 1 and 2 and note also column 1, line 57 to column 2, line 53 and column 3, lines 12-14.

8. Claims 1-23 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sachs et al (U.S. '846).

The reference discloses a cache memory apparatus as in the claimed invention. See, for example, the cache random access memory; the host processor port/bus and system port/bus; and the CPU and system interfaces including input and output register circuits shown in Figures 8, 20 and 21, as well as column 19, lines 48+ and column 33, lines 27+. Note also that the mere labelling of a register (such as an "update" or "miss (hit)" register) without a recitation of its function or operation does not render the claimed invention patentably distinct. The input and output data and address registers disclosed in the reference anticipate the registers as broadly set forth in the claims.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Glier is cited as teaching a shared memory arrangement including system and host ports as in the claimed invention.

Cutts, Jr. et al is cited as teaching a data processing system having a cache memory, read and write buffers/registers and bypass "means" as in the claimed invention.

Calle et al is cited as disclosing an input/output system having a cache memory and bypass "means" similar to the claimed invention.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2312

EXHIBIT 11

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/678,912	04/01/91	CHAN	A M-1018-1P-US

GOSSAGE,J

EXAMINER

E3M1/1122

B. NOEL KIVLIN
SKJERVEN, MORRILL, MACPHERSON,
FRANKLIN & FRIEL
25 METRO DRIVE, SUITE 700
SAN JOSE, CA 95110

ART UNIT	PAPER NUMBER
2312	13

DATE MAILED: 11/22/94

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on 8-11-94 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ~~days~~ from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 1-27 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☐ Claims _____ are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☑ The proposed drawing correction, filed 8-11-94, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev.9-89)

1. Receipt is hereby acknowledged of the declaration filed August 11, 1994, which declaration has been placed of record in the file. It is noted here that the substitute declaration was signed December 23, 1993 after the application was amended in ~~as~~ an amendment filed on September 9, 1993. Although the substitute declaration does not refer to the amendment, this does not appear to be an explicit requirement under 37 CFR 1.63 and, thus, the substitute declaration is deemed acceptable (the declaration adequately identities the application to which it is directed).

2. The Abstract of the Disclosure is objected to because in (page) lines 7-8, it appears "A... system" should be -- The ... apparatus -- for clarity and consistency.

Also, the abstract should be rewritten as a single paragraph including all changes made to date to avoid possible confusion and mistake during the printing and issue process, should any patent issue based on this application.

Correction is required. See M.P.E.P. § 608.01(b).

3. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on August 11, 1994 have been approved by the Examiner, subject to drafting review.

Applicant should submit a complete set of all proposed changes to date to ensure that the Examiner and applicant are in agreement on the changes to be made. Again note MPEP 608.02(r) and (v).

It is also noted that the label/designation "ads#" within step 300 in Fig. 53 is not adequately clear. It also is not entirely clear to what the label "assert: brdy# ..." (near step 308 in Figure 53) refers.

Clarification by way of explanation and/or amendment is required. [Note that this issue was not adequately addressed in applicant's remarks filed August 11, 1994 (at page 7). See the Office action mailed March 8, 1994 at page 4, lines 18-2. Does this refer to the cache?]

4. The disclosure is objected to because of the following informalities:

On page 15, line 1, "if" should be -- of --.

On page 43, line 1, "8" should be -- 8A-8C --.

In claim 24, line 16, "a" should be -- an --.

Appropriate correction is required.

5. Claims 13 and 27 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13, it remains unclear how simply "validating data" itself prevents the writing of data into RAM. See also the Office Action mailed March 8, 1994, at page 7, lines 1-4 and note that no response was apparently made to this issue.

In claim 27, the antecedents for "said input (output) data"

are not entirely clear since there is more than one input (output) data set forth in claim 24.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 4, 6-8 and 13-15 are rejected under 35 U.S.C. § 102(b) as being anticipated by Malinowski.

Again, the broad claim language "reads on" the structure disclosed by the reference. Here, the write registers 30 and 32 are input registers and the read registers 40 and 42 constitute "output registers." The outputs of the read registers and MUX 44 may be broadly considered a "system" port, with the inputs to MUX 34 and the write registers serving as the "host port." See Figures 1 and 2 and note also column 1, line 57 to column 2, line 53 and column 3, lines 12-14.

7. Claims 1-27 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sachs et al (U.S. '846).

Sachs et al (U.S. '846) discloses a cache memory apparatus

as in the claimed invention. See, for example, the cache random access memory; the host processor port/bus and system port/bus; and the CPU and system interfaces including input and output register circuits shown in Figures 8, 20 and 21, as well as column 19, lines 48+ and column 33, lines 27+. Note also that the mere labelling of a register (such as an "update" or "miss (hit)" register) without a recitation of its function or operation does not render the claimed invention patentably distinct. The input and output data and address registers disclosed in the reference anticipate the registers as broadly set forth in the claims.

8. Applicant's arguments filed August 11, 1994 have been considered but are not persuasive. While the Examiner recognizes that the references do not depict the same embodiments as those disclosed by applicant, the broad nature of the claim language is such that the claims "read on" the structures shown by the references as noted above. Applicant has not adequately addressed the explanation provided by the Examiner of how the claimed "system port," "host port," "input registers," and "output registers" are met by the references. Again note that the mere labelling of a register (such as an "update" register) without a clear recitation of its function or operation does not render the claimed invention patentably distinct. The functional language "the writing ... and ... providing of data ...

'allowing' the host port to be decoupled" is not sufficient to patentably define the claimed invention over the prior art.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2312

G. Gossage/kw
November 21, 1994

EXHIBIT 12

23X 5-15-91 030 Popek

L:\M\1018\1P\O\PAMD.BNK

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alfred K. Chan

Assignee: MOS Electronics, Inc.

Title: RANDOM ACCESS CACHE MEMORY

Serial No.: 07/678,912 Filed: April 1, 1991

Examiner: Group Art Unit: 233

Attorney Docket No.: M-1018-1P US

San Jose, California
October 18, 1991

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application filed April 1, 1991 as follows.

IN THE CLAIMS

Please amend Claims 1, 3, and 5 as follows:

1. (Amended) A memory cache apparatus comprising:

a random access memory;

a host port;

a system port;

an input latch coupled to said host port for selectively writing data to said memory; and

an output register coupled to said system port for receiving data from said memory and selectively furnishing said data to [a selected one of said host port and] said system port.

3. (Amended) An apparatus as in Claim 2, wherein said input latch is a memory write register, said input register is

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an update register, and said output register [comprises a read hold register for furnishing data to said host port and] is a write back register for furnishing data to said system port.

5. (Amended) The memory cache apparatus as recited in Claim 4 further comprising:

a miss address register coupled to said random access memory for storing [output] an addressing [signals] signal corresponding to said output data; and

a hit address register coupled to said miss address register for storing [input] an addressing [signals] signal corresponding to said input data.

Please add new Claims 6 - 18 as follows:

6. (New) The memory cache apparatus as recited in Claim 1 further comprising a second output register coupled to said random access memory and to said host port for furnishing data from said memory to said host port.

7. (New) The memory cache apparatus as recited in Claim 6 wherein said second output register is a read hold register.

8, (New) The memory cache apparatus as recited in Claim 6 wherein said input register can store a plurality of words of data.

9. (New) The memory cache apparatus as recited in Claim 8 further comprising means for masking the writing of selected words of data into said random access memory.

10. (New) The memory cache apparatus as recited in Claim

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1 further comprising a bypass path coupled between said host port and said system port for directly allowing the passage of data between said host port and said system port.

11. (New) The memory cache apparatus as recited in Claim 5 further comprising a counter coupled to said miss address register.

12. (New) The memory cache apparatus as recited in Claim 11 wherein said counter increments from an address associated with a first line of data to a subsequent line of data.

13. (New) The memory cache apparatus as recited in Claim 2 further comprising means for validating data stored within said input register to selectively prevent the writing of data of said data stored within said input register into said random access memory.

14. (New) The memory cache apparatus as recited in Claim 1 wherein said random access memory includes a plurality of parity bits.

15. (New) The memory cache apparatus as recited in Claim 1 wherein said RAM is organized in a plurality of lines wherein each of said lines comprises a plurality of word storage locations, and wherein each of said word storage locations is selectively writable.

16. (New) The memory cache apparatus as recited in Claim 1 wherein said random access memory is single ported.

17. (New) The memory cache apparatus as recited in Claim

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16 wherein said random access memory has a wider bandwidth than said host port and said system port.

18. (New) The memory cache apparatus as recited in Claim 1 wherein said random access memory performs a read-modify-write operation.

REMARKS

Applicant requests the Examiner to amend Claims 1, 3 and 5 and to add Claims 6-18 as indicated above. Examination and allowance of the pending claims is requested.

Respectfully submitted,

B. Noël Kivlin
Agent for Applicant
Reg. No. 33,929

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on 10-18 19 91

10-18-91
Date of Signature

Agent for Applicant

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EXHIBIT 13

GP 2312

PATENT

#7/B
W. Lawson
12/30/93

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alfred K. Chan

Assignee: MOS Electronics, Corp.

Title: RANDOM ACCESS CACHE MEMORY

Serial No: 07/678,912 Filed: 04-01-91

Examiner: Glenn Gossage Group Art Unit: 2312

Attorney Docket No: M-1018-1P US

San Jose, California
November 18, 1993

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C.

AMENDMENT

Dear Sir:

Responsive to the Office Action mailed on September 9, 1993, kindly amend the above-identified application as follows:

In the Title:

Please delete "CACHE".

Please add --~~DUAL PORTED~~ CACHE INCLUDING A-- before "RANDOM".

Please add --AND DECOUPLING CIRCUITS-- after "MEMORY".

In the Abstract:

In line 4, change --The-- to "A".

In line 5, change --the-- to "a".

Please delete lines 19 - 28.

CS14031 12/23/93 07678912 19-2386 140 103 66.00CH

B

In the Drawings:

Please amend the drawings as shown in red on the attached sheets.

In the Specification:

On page 1, line 6, please add --, now abandoned--after "1990".

On page 2, line 21, please add (a "#" indicates an active low signal throughout the specification) after "ads#".

On page 7, line 30, please add --using a cache memory in accordance with the present invention-- after "computer system".

On page 7, line 32, please add --using a cache memory in accordance with the present invention-- after "computer system".

On page 7, line 34, please change "Figure 8 is" to --Figures 8A, 8B and 8C, which are generally referred to as Figure 8 throughout the specification, are--

On page 19, line 34, please change "associates with" to --is associated with--.

On page 19, line 35, please change "associates with" to --is associated with--.

On page 19, line 36, please change "associates with" to --is associated with--.

On page 19, line 37, please change "associates with" to --is associated with--.

On page 37, line 17, please change "controller" to --Controller--.

On page 114, line 30, please change "57" to --58--.

In the Claims:

Please amend claims 1 - 18 as follows:

1. (Twice Amended) A cache memory [cache] apparatus comprising:

a random access memory;

a host port;

a system port;

a[n] first input register [latch coupled to said host port] for selectively writing data to said random access memory, said first input register being coupled between said host port and said random access memory; and

an output register [coupled to said system port] for receiving data from said random access memory and selectively providing [furnishing said] data to said system port, said output register being coupled between said random access memory and said system port.

2. (Amended) An apparatus as in claim 1, further comprising a[n] second input register [connected to said system port] for [furnishing] providing data to said memory, said second input register being coupled between said random access memory and said system port.

3. (Twice Amended) An apparatus as in Claim 2, wherein said first input [latch] register is a memory write register, said second input register is an update register, and said output register is a write back register for [furnishing] providing data

to said system port.

4. A cache memory [cache] apparatus comprising:
a random access memory;
a host port;
a system port;
an input register coupled to said random access memory for selectively writing input data to said random access memory; and
an output register coupled to said system port for receiving output data from said random access memory and selectively furnishing said output data to said system port;
wherein said input data is [written into] provided to said random access memory from said input register at the same time [when] that said output data is provided by [furnished to said system port from] said output register to said system port.

5. (Twice Amended) The cache memory [cache] apparatus as recited in Claim 4 further comprising:
a miss address register coupled to said random access memory for storing an address[ing] signal corresponding to a word of said output data; and
a hit address register coupled to said miss address register for storing an address[ing] signal corresponding to a word of said input data.

6. (Amended) The cache memory [cache] apparatus as recited in Claim 1 further comprising a second output register coupled [to] between said random access memory and [to] said host port for [furnishing] providing data from said random access memory to said host port.

7. (Amended) The cache memory [cache] apparatus as recited in Claim 6 wherein said second output register is a read hold register.

8. (Amended) The cache memory [cache] apparatus as recited in Claim 6 wherein said second input register can store a plurality of words of data.

9. (Amended) The cache memory [cache] apparatus as recited in Claim 8 further comprising means for masking [the] writing of selected words of data into said random access memory.

10. (Amended) The cache memory [cache] apparatus as recited in Claim 1 further comprising a bypass path coupled between said host port and said system port for directly allowing [the] passage of data between said host port and said system port.

11. (Amended) The cache memory [cache] apparatus as recited in Claim 6 further comprising a counter coupled to said miss address register.

12. (Amended) The cache memory [cache] apparatus as recited in Claim 11 wherein said counter increments from an address associated with a first line of data to an address associated with a subsequent line of data.

13. (Amended) The cache memory [cache] apparatus as recited in Claim 2 further comprising means for validating data stored within said second input register to selectively prevent the writing [of data] of said data stored within said second input register into said random access memory.

14. (Amended) The cache memory [cache] apparatus as recited

in Claim 1 wherein said random access memory includes storage for a plurality of parity bits.

15. (Amended) The cache memory [cache] apparatus as recited in Claim 1 wherein said [RAM] random access memory is organized in a plurality of lines wherein each of said lines comprises a plurality of word storage locations, and wherein each of said word storage locations is selectively writable.

16. The cache memory [cache] apparatus as recited in Claim 1 wherein said random access memory is single ported.

17. (Amended) The cache memory [cache] apparatus as recited in Claim 16 wherein said random access memory [has] is accessed with a wider bandwidth than said host port and said system port.

18. (Amended) The cache memory [cache] apparatus as recited in Claim 1 wherein said random access memory [performs] is written using a read-modify-write operation.

Please add the following new claims:

19. (New) A cache memory apparatus comprising:
a random access memory;
a host port;
a system port;
a first input register for selectively writing input data to said random access memory, said first input register being coupled between said host port and said random access memory;
a first output register for selectively furnishing output data to said system port, said first output register being coupled between said random access memory and said system

port, said input data being provided to said random access memory from said first input register at the same time that said output data is provided by said first output register to said system port;

a second input register for providing second input data to said random access memory, said second input register being coupled between said random access memory and said system port; and,

a second output register coupled between said random access memory and said host port for providing second output data from said random access memory to said host port, said second input data being provided to said random access memory from said second input register at the same time that said second output data is provided by said second output register to said system port.

20. (New) An apparatus as recited in claim 17 further comprising a bypass path coupled between said host port and said system port for directly allowing passage of data between said host port and said system port.

21. (New) An apparatus as recited in Claim 19, wherein said first input register is a memory write register, said second input register is an update register, said first output register is a write back register, and said second output register is a read hold register.

22. (New) The cache memory apparatus as recited in Claim 19 wherein said second input register can store a plurality of words of data.

23. (New) The cache memory apparatus as recited in Claim 21 further comprising means for masking writing of selected words of

B8 Cont. data into said random access memory.

REMARKS

The declaration has been set forth as being defective for not including the statement that the person making the declaration has reviewed and understands the contents of the specification, including the claims. This rejection is respectfully traversed.

The inventor states in the declaration which was executed for the above-identified application, in part, that "I have reviewed and understand the contents of the above identified application . . . ." An application, as set forth by 37 C.F.R. §1.51, includes "(1) a specification, including a claim or claims . . . ." Accordingly, a declaration which sets forth that the inventor has reviewed and understands the contents of an application satisfies the requirement of 37 C.F.R. §1.63(b)(1).

Responsive to the Examiner's objection to the Title of the Invention, the Title has been amended to be more descriptive. Responsive to the Examiner's objection to the Abstract of the Disclosure, the Abstract of the Disclosure has been amended.

Responsive to the Examiner's objection to the drawings, the drawings have been amended to correct the objections set forth by the Examiner. Regarding the Examiner's comment about the darkened triangular symbol, the application sets forth on pages 46 and 47 that the data path drivers are designated with solid triangular symbols.

Responsive to the Examiner's objection to the specification, the specification has been amended to correct the errors set forth by the Examiner.

Claims 1 - 18 stand rejected under 35 U.S.C. §103 over "applicant's admitted prior art" in view of either Aichelmann, Jr. et al. or Watanabe. This rejection is respectfully traversed.

The present invention relates to providing a cache memory system which decouples a main memory subsystem from a host data bus. More specifically, the present invention, as set forth in independent claim 1, relates to a cache memory which includes a random access memory, a host port, a system port, an input register coupled between the host port and the random access memory and an output register coupled between the system port and the random access memory. The input register selectively provides data to the random access memory. The output register receives data from the random access memory and selectively provides the data to the system port. By selectively providing the data to and from the random access memory, it is possible to effectively decouple to host port from the system port and thus to decouple the buses that are connected to these ports. Independent claim 4 is of similar scope but adds the further limitation that the input data is provided to the random access memory from the input register at the same time that the output data is provided by the output register to the system port. New independent claim 19 is of similar scope but adds the further limitations of a second input register which provides second input data to the random access memory and is coupled between the random access memory and the system port, a second output register which provides second output data to the host port and is coupled between the random access memory and the host port and a bypass path which is coupled between the host port and the system port for directly allowing passage of data between the host port and the system port.

The Background of the Invention section of the present application sets forth with reference to Figure 4 that it was known

to provide an external cache which is connected to a local address bus and a local data bus. A cache controller, which determines whether data corresponding to a particular address is resident in the cache memory, is coupled to the local address bus as well as a local control bus. If the particular address is not resident in the cache then the address and data are transferred via cache bus buffers 32A and 32B, respectively, to system bus 34. Cache bus buffer/latches 32A and 32B are controlled by cache bus controller 36 which receives control information from cache controller 30. This discussion does not set forth that a memory apparatus which includes a host port and a system port is prior art.

Watanabe discloses a cache memory having a dual ported tag storage section which allows the cache to be independently accessible by a processor as well as by another cache. The dual ported tag storage section saves tag addresses and valid tag address information corresponding to respective data storage locations in a data storage section of the cache and provides hit indication signals to the data storage section of the cache. One of the ports of the dual ported tag storage section is coupled to the processor and allows the processor to write to and read from the data storage section of the cache memory. The other port of the dual ported tag section is coupled to a system bus and allows determination of whether information which was updated by another cache is stored in the cache memory by comparing the address tags which are stored in the tag storage section. If the information was updated, then this storage location is invalidated by clearing the valid tag address information which corresponds to this address. Such a system provides advantages in a multiprocessing system in which each of the processors includes a respective dedicated cache. Watanabe also discloses as prior art a cache memory which has a first I/O buffer that is coupled to a central processing unit and another I/O buffer that is coupled to a system

bus. The I/O buffers temporarily hold data that is subsequently delivered to the processor, the main memory or the data storage section.

Aichelmann, Jr. et al. discloses an intermediate buffer memory which includes both a serial port which is coupled to lower levels of memory and a parallel port which is coupled to higher levels of memory. The parallel port is coupled with a storage array via a parallel bank of AND gates which provide a chip select and read/write enabling. The serial port is coupled to the storage array via a buffer which buffers the serial signal; the buffer is coupled in parallel to the store array. Data transfers with the higher memory level are performed in parallel while data transfers with the lower memory level are performed in serial. By using the buffer, data transfer between the serial port and the buffer may be performed concurrently with data transfer between the memory array and the parallel port.

The "cited prior art", Watanabe, and Aichelmann, Jr. et al. do not disclose or suggest, taken alone or combination, a cache memory which includes both an input register which is coupled between a host port and a random access memory and which selectively provides data to the random access memory and an output register which receives data from the random access memory and selectively provides the data to the system port, as required by independent claim 1. Additionally, the "cited prior art", Watanabe, and Aichelmann, Jr. et al. do not disclose or suggest, taken alone or combination, the further limitation of the input data being provided to the random access memory from the input register at the same time that the output data is provided by the output register to the system port, as required by independent claim 4. Additionally, the "cited prior art", Watanabe, and Aichelmann, Jr. et al. do not disclose or suggest, taken alone or combination, the

further limitations of a second input register which provides second input data to the random access memory and is coupled between the random access memory and the system port, a second output register which provides second output data to the host port and is coupled between the random access memory and the host port and a bypass path which is coupled between the host port and the system port for directly allowing passage of data between the host port and the system port, all as required by new independent claim 19.

Claims 2, 3, 6 - 10, and 13 - 18 depend from claim 1 and are allowable with it. Claims 4, 11 and 12 depend from claim 4 and are allowable with it.

In summary, a new declaration has been filed to address the Examiner's objection to the Declaration. The Title, Specification, Drawings, and Abstract have been amended to address the Examiner's objections. Additionally, the rejection under 35 U.S.C. §103 over "the cited prior art" in view of Aichelmann, Jr. et al. or Watanabe has been traversed.

Accordingly, the application is now in condition for allowance, and such allowance is respectfully solicited.

Respectfully submitted,

Stephen A. Terrile
Attorney for Applicant(s)
Reg. No. 32,946

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on December 2, 1993.

12/2/93
Date of Signature

Attorney for Applicant(s)

EXHIBIT 14

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alfred K. Chan

Assignee: MOS Electronics, Corp.

Title: RANDOM ACCESS CACHE MEMORY

Serial No: 07/678,912 Filed: 04-01-91

Examiner: Glenn Gossage Group Art Unit: 2312

Attorney Docket No: M-1018-1P US

San Jose, California
August 8, 1994

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C.

AMENDMENT

Dear Sir:

Responsive to the Office Action mailed on March 8, 1994, kindly amend the above-identified application as follows:

In the Title:

Please change "A RANDOM ACCESS MEMORY AND DECOUPLING" to --DECOUPLING REGISTER--.

Please delete "DUAL PORTED"

P 30182 08/23/94 07678912 19-2386 030 102 74.00CH
P 30183 08/23/94 07678912 ~~19-2386 030 102~~ 88.00CH

In the Abstract:

In line 6, after "transfers", please insert

--The memory cache apparatus includes a random access memory, a host port, and a system port. The memory cache apparatus further includes an input register connected to the host port for selectively writing data to the random access memory and an output register connected to the system port for receiving data from the random access memory and selectively furnishing the data to the

host port or the system port. In one embodiment, the input register is a memory write register, and the output register includes a read hold register and a write back register.

In lines 8 and 11, please change "from the" to --from a--.

In lines 6 and 7, please delete "In burst mode, a 'demand word first' wrapped around quad fetch order is supported."

In the Drawings:

Please amend the Figs. 8A - 8C and Figs. 53 - 58 of the drawings as shown in red on the attached sheets.

In the Specification:

On page 12, line 17, please change "Figure 8" to --Figures 8A-8C--.

On page 15, line 1, please change "Figure 8" to --Figures 8A-8C--.

On page 15, line 8, please change "Figure 8" to --Figures 8A-8C--.

On page 16, line 12, please change "Figure 8" to --Figures 8A-8C--.

On page 18, line 5, please change "Figure 8" to --Figures 8A-8C--.

On page 18, line 25, please change "Figure 8" to --Figures 8A-8C--.

On page 19, lines 34 - 37 please change

"BE3# associates with D<31:24>
BE2# associates with D<23:16>
BE1# associates with D<15:8>
BE0# associates with D<7:0>"

to

BE3# is associated with D<31:24>
BE2# is associated with D<23:16>
BE1# is associated with D<15:8>
BE0# is associated with D<7:0>

On page 46, line 32, please change "Figure 8" to --Figures 8A-8C--.

In the Claims:

Please amend claims 1, 4 and 19 as follows:

1. (Three Times Amended) A cache memory apparatus comprising:
a random access memory;
a host port;
a system port;
a first input register for selectively writing data to said random access memory, said first input register being coupled between said host port and said random access memory; and
an output register for receiving data from said random access memory and selectively providing data to said system port, said output register being coupled between said random access memory and said system port,
the selective writing of data to said random access memory and the selective providing of data to said system port allowing said host port to be decoupled from said system port.

4. (Twice Amended) A cache memory apparatus comprising:
a random access memory;
a host port;
a system port;
an input register coupled to said random access memory for selectively writing input data to said random access memory; and

an output register coupled to said system port for receiving output data from said random access memory and selectively [furnishing] providing said output data to said system port;

wherein said input data is provided to said random access memory from said input register at the same time that said output data is provided by said output register to said system port, the selective writing of data to said random access memory and the selective providing of data to said system port allowing said host port to be decoupled from said system port.

19. (Amended) A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a first input register for selectively writing input data to said random access memory, said first input register being coupled between said host port and said random access memory;

a first output register for selectively furnishing output data to said system port, said first output register being coupled between said random access memory and said system port, said input data being provided to said random access memory from said first input register at the same time that said output data is provided by said first output register to said system port, the selective writing of data to said random access memory and the selective furnishing of data to said system port allowing said host port to be decoupled from said system port;

a second input register for providing second input data to said random access memory, said second input register being coupled between said random access memory and said system port; and,

a second output register coupled between said random access memory and said host port for providing second output data from said random access memory to said host port, said second input data being provided to said random access memory from said second input register at the same time that said second output data is provided by said second output register to said system port.

Please add the following new claims:

24. (New) A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a memory write register for selectively writing input data to said random access memory, said memory write register being coupled between said host port and said random access memory;

a write back register for selectively furnishing output data to said system port, said write back register being coupled between said random access memory and said system port, said input data being provided to said random access memory from said memory write register at the same time that said output data is provided by said write back register to said system port;

a update register for providing second input data to said random access memory, said update register being coupled between said random access memory and said system port;

a read hold register coupled between said random access memory and said host port for providing second output data from said random access memory to said host port, said second input data being provided to said random access memory from said update register at the same time that said

second output data is provided by said read hold register to said system port; and

a bypass path coupled between said host port and said system port for directly allowing passage of data between said host port and said system port.

25. (New) The cache memory apparatus as recited in Claim 24 wherein said update register can store a plurality of words of data.

26. (New) The cache memory apparatus as recited in Claim 24 further comprising means for masking writing of selected words of data into said random access memory.

27. (New) The cache memory apparatus as recited in Claim 24 further comprising:

a miss address register coupled to said random access memory for storing an address signal corresponding to a word of said output data; and

a hit address register coupled to said miss address register for storing an address signal corresponding to a word of said input data.

REMARKS

The Declaration has been set forth as being defective for not including the statement that the person making the declaration has reviewed and understands the contents of the specification, including the claims. A newly executed declaration in compliance with 37 C.F.R. §1.67(a) is enclosed with this response.

Responsive to the Examiner's objection to the Title of the Invention, the Title has been amended to be more descriptive.

Responsive to the Examiner's objection to the Abstract of the Disclosure, the Abstract of the Disclosure has been amended.

Responsive to the Examiner's objection to the drawings, the drawings have been amended to correct the objections set forth by the Examiner. Support for the amendments to Figs 8A - 8C can be found at pages 46 - 48. Support for the amendments to Figs. 53 - 56 can be found at page 109, line 13 to page 114, line 5. Support for the amendments to Figs. 57 and 58 can be found at page 114, line 6 to page 115, line 14.

Responsive to the Examiner's objection to the specification, the specification has been amended to correct the errors set forth by the Examiner.

Claims 1 - 18 stand rejected under 35 U.S.C. §102(b) over Malinowski and under 35 U.S.C. §102(e) over Sachs et al. These rejections are respectfully traversed.

The present invention relates to providing a cache memory system which decouples a main memory subsystem from a host data bus. More specifically, the present invention, as set forth in independent claim 1, relates to a cache memory which includes a random access memory, a host port, a system port, an input register coupled between the host port and the random access memory and an output register coupled between the system port and the random access memory. The input register selectively provides data to the random access memory. The output register receives data from the random access memory and selectively provides the data to the system port. By selectively providing the data to and from the random access memory, it is possible to effectively decouple to host port from the system port and thus to decouple the buses that are connected to these ports. Independent claim 4 is of similar scope but adds the further limitation that the input data is

provided to the random access memory from the input register at the same time that the output data is provided by the output register to the system port. Independent claim 19 is of similar scope but adds the further limitations of a second input register which provides second input data to the random access memory and is coupled between the random access memory and the system port, a second output register which provides second output data to the host port and is coupled between the random access memory and the host port. New independent claim 24 is of similar scope but adds the further limitation of a bypass path which is coupled between the host port and the system port for directly allowing passage of data between the host port and the system port.

Malinowski discloses a memory which includes registers coupled between read and write ports of the memory array and input and output ports of the memory. More specifically, Malinowski discloses a first in first out (FIFO) memory which includes two pairs of cache registers. One pair, a write pair, are coupled between a data input port and the memory array write port. The other pair, a read pair, are coupled between the data out port and the memory read port. Malinowski also discloses a last in first out (LIFO) memory which includes only a single pair of cache registers. One of the LIFO cache registers is coupled between the data in/out port and the read port of the memory and the other LIFO cache register is coupled between the data in/out port and the write port of the memory. Malinowski sets forth that the technique used for the LIFO memory may also be used in a random access memory. With a random access memory, a speed advantage is achieved whenever sequential reads or all writes from/to the RAM array are performed. Extra address comparators compare externally applied addresses with the addresses generated internally and if a hit is indicated, one of the desired read/write functions would be performed. In the case of a miss, an extra wait state signal goes high to indicate to the processor that an extra clock cycle has to

be wasted to decode the out of sequence address and get the data. In the case of all writes, both data and address are cached for the next cycle memory array writes. (Col. 8, lines 16 - 36.)

Sachs et al. discloses a cache memory management unit which includes a cache memory subsystem 220 which is coupled to a cache bus via cache output register 230 and cache input register 240 and is coupled to a system bus via system bus input register 260 and system bus output register 250. The cache output register is directly coupled via a data out line to the memory subsystem. The cache input register, system bus input register and system bus output register are coupled to the memory subsystem via a data bus 241.

Malinowski and Sachs et al. do not disclose or suggest, taken alone or in combination, a cache memory which includes both an input register which is coupled between a host port and a random access memory and which selectively provides data to the random access memory and an output register which receives data from the random access memory and selectively provides the data to the system port, as required by independent claim 1. Additionally, Malinowski and Sachs et al. do not disclose or suggest, taken alone or in combination, the further limitation of the input data being provided to the random access memory from the input register at the same time that the output data is provided by the output register to the system port, as required by independent claim 4. Additionally, Malinowski and Sachs et al. do not disclose or suggest, taken alone or in combination, the further limitations of a second input register which provides second input data to the random access memory and is coupled between the random access memory and the system port, a second output register which provides second output data to the host port and is coupled between the random access memory and the host port, all as required by independent claim 19. Additionally, Malinowski and Sachs et al. do

not disclose or suggest, taken alone or in combination, the further limitation of a bypass path which is coupled between the host port and the system port for directly allowing passage of data between the host port and the system port, all as required by independent claim 19.

Claims 2, 3, 6 - 10, and 13 - 18 depend from claim 1 and are allowable with it. Claims 4, 11 and 12 depend from claim 4 and are allowable with it. New claims 25 - 28 depend from new independent claim 24 and are allowable with it.

In summary, a new declaration has been filed to address the Examiner's objection to the Declaration. The Title, Specification, Drawings, and Abstract have been amended to address the Examiner's objections. Additionally, the rejection under 35 U.S.C. §102(b) over Malinowski and the rejection under 35 U.S.C. §102(e) over Sachs et al. have been traversed.

Accordingly, the application is now in condition for allowance, and such allowance is respectfully solicited.

Respectfully submitted,

Stephen A. Terrile
Attorney for Applicant(s)
Reg. No. 32,946

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on 8/8, 1994.

8/8/94
Date of Signature

Attorney for Applicant(s)

EXHIBIT 15

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alfred K. Chan

Assignee: MOS Electronics Corporation

Title: CACHE INCLUDING DECOUPLING REGISTER CIRCUIT (AS AMENDED)

Serial No: 07/678,912 Filed: 04-01-91

Examiner: G. Gossage Group Art Unit: 2312

Attorney Docket No: M-1018-1P US

San Jose, California
April 7, 1995

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C.

RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

This paper is in response to the Office Action mailed November 22, 1994 having a shortened statutory period set to expire February 22, 1995. Accompanying this response is a petition to extend the shortened statutory period by two months, setting a new time for response of April 24, 1995 (April 22 being a Saturday and April 23 being a Sunday). Further examination and reconsideration are respectfully requested in view of the amendments and remarks set forth below.

PROVISIONAL PETITIONS

The Office is provisionally petitioned to extend the shortened statutory period as necessary to avoid abandonment of the Application in relation to the outstanding Office action. If appropriate, a separate Petition for Extension accompanies this Response, this provisional petition being effective in the event that the separate Petition for Extension is defective or

missing. The Office is provisionally authorized to charge any amount required to avoid abandonment of the Application in relation to the outstanding Office action to account number 19-2386. A separate Fee Transmittal accompanies this Response, this provisional fee authorization being effective in the event that the separate Fee Transmittal is defective or missing.

AMENDMENT

In the Abstract

In **lines 7-8**, please change "A cache memory system" to --The memory cache apparatus--.

In the Specification

On **page 15, line 1**, please change "if" to --of--.

On **page 15, line 1**, please change "8" to --8A-8C--.

In the Claims

Please cancel claims 3 and 7. Also, kindly amend claims 1, 2, 4-6, 8, 9, 13, 19, and 21-27, as follows:

1. (Four Times Amended) A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a [first input] memory write register for buffering first data received from said host port and selectively [writing] providing the first data to one of said random access memory, said system port, and said random access memory and said system port, said [first input] memory write register being coupled between said host port and said random access memory and between said host port and said system port; and

[an output] a write back register for holding second data received [receiving data] from said random access memory and selectively providing the second data to said system port, said [output] write back register being coupled between said random access memory and said system port[,];

wherein the buffering and selective [writing] providing of the first data to said random access memory and the holding and selective providing of the second data to said system port [allowing] allows memory accesses at said host port to be decoupled from memory accesses at said system port.

91. (Twice Amended) An apparatus as in claim 1, further comprising [a second input] a memory update register for holding fetched data and providing the fetched data to said random access memory, said [second input] memory update register being coupled between said random access memory and said system port, wherein the holding and selective providing of the second data and the holding of the fetched data allows write back and fetch operations at said system port to be decoupled from said random access memory.

B1. (Three Times Amended) A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

[an input] a memory write register coupled to said random access memory, to said host port, and to said system port for buffering and selectively [writing] providing input data received from said host port to one of said random access memory, said system port, and said random access memory and said system port;

and

[an output] a write back register coupled to said system port and to said random access memory for [receiving] holding output data received from said random access memory and selectively providing said output data to said system port;

wherein [said] the input data is provided to said random access memory from said [input] memory write register at the same time that [said] the output data is provided by said [output] write back register to said system port, the buffering and selective [writing] providing of the input data to said random access memory and the holding and selective providing of the output data to said system port allowing memory accesses at said host port to be decoupled from memory accesses at said system port.

14. (Three Times Amended) The cache memory apparatus as recited in Claim 13 further comprising:

a miss address register coupled to said host port and to said random access memory for storing a[n] cache miss address signal corresponding to a word of [said] the output data to be received from said random access memory into said write back register; and

a hit address register coupled to said host port and to said [miss address register] random access memory for storing a[n] cache hit address signal [corresponding to] selective for a word [of said input data] stored in said random access memory.

87. (Twice Amended) The cache memory apparatus as recited in Claim 1 further comprising a [second output] read hold register coupled between said random access memory and said host port for buffering and providing burst read data from

said random access memory to said host port.

11 8. (Twice Amended) The cache memory apparatus as recited in [Claim 6] Claim 9 wherein said [second input] memory update register can store a plurality of words of the fetched data.

12 9. (Twice Amended) The cache memory apparatus as recited in Claim 11 8 further comprising means for masking [writing] the providing of selected ones of said words of the fetched data [into] to said random access memory.

10 13. (Twice Amended) The cache memory apparatus as recited in Claim 9 7 further comprising means for [validating] identifying ones of the fetched data [stored within] held in said [second input] memory update register [to selectively prevent the writing of said data stored within] as not corresponding to ones of the second data held in said write back register for write back to said system port, said identifying means being selective for the ones of the fetched data to be provided from said [second input] memory update register [into] to said random access memory.

17 19. (Twice Amended) A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a [first input] memory write register for buffering and selectively writing first input data to said random access memory, said [first input] memory write register being coupled between said host port and said random access memory;

a [first output] write back register for holding and selectively furnishing first output data to said

system port, said [first output] write back register being coupled between said random access memory and said system port, [said] the first input data being provided to said random access memory from said [first input] memory write register at the same time that [said] the first output data is provided by said [first output] write back register to said system port, the selective writing of the first input data to said random access memory and the selective furnishing of the first output data to said system port allowing memory accesses at said host port to be decoupled from memory accesses at said system port;

a [second input] memory update register for holding and selectively providing second input data to said random access memory, said [second input] memory update register being coupled between said random access memory and said system port, wherein the holding and selective furnishing of the first output data and the holding and selective providing of the second input data allows write back and memory update operations at said system port to be decoupled from said random access memory; and,

a [second output] read hold register coupled between said random access memory and said host port for providing second output data from said random access memory to said host port, [said] the second input data being provided to said random access memory from said [second input] memory update register at the same time that [said] the second output data is provided by said [second output] read hold register to said [system] host port.

20 21. (Amended) An apparatus as recited in Claim 19, wherein [said] the first input [register is a] data comprises memory write [register] data, [said] the second input [register is an update register] data comprises system fetch data, [said] the first output [register is a] data comprises system write back [register] data, and [said] the second output [register is a read hold register] comprises burst read data.

19 22. (Amended) The cache memory apparatus as recited in Claim 17 wherein said [second input] memory update register can store a plurality of words of the second input data.

21 23. (Amended) The cache memory apparatus as recited in Claim 20 further comprising means for masking writing of selected words of the system fetch data into said random access memory.

22 24. (Amended) A cache memory apparatus comprising:

a random access memory;

a host port;

a system port;

a bypass path coupled between said host port and said system port for directly passing data between said host port and said system port;

a memory write register for buffering and selectively [writing input] providing memory write data to one of said random access memory, said system port via said bypass path, and said random access memory and said system port via said bypass path, said memory write register being coupled to said bypass path and between said host port and said random access memory;

a write back register for holding and selectively

furnishing [output] write back data to said system port, said write back register being coupled between said random access memory and said system port, said write back register allowing the write back data to be furnished to said system port at the same time that said memory write register provides [said input] the memory write data [being provided] to said random access memory [from said memory write register at the same time that said output data is provided by said write back register to said system port];

a memory update register for holding and selectively providing [second input] system fetch data to said random access memory, said memory update register being coupled between said random access memory and said system port, wherein the holding and selective furnishing of the write back data and the holding and selectively providing of the system fetch data allows write back and memory update operations at said system port to be decoupled from said random access memory; and

a read hold register coupled between said random access memory and said host port for buffering and providing [second output] burst read data from said random access memory to said host port, said read hold register allowing the burst read data to be provided to said host port at the same time that said memory update register provides [said second input] the system fetch data [being provided] to said random access memory [from said update register at the same time that said second output data is provided by said read hold register to said system port; and

a bypass path coupled between said host port and said system port for directly allowing passage of data between said host port and said system port].

23 25. (Amended) The cache memory apparatus as recited in Claim 22 wherein said memory update register can store a plurality of words of the system fetch data.

24 26. (Amended) The cache memory apparatus as recited in Claim 22 further comprising means for masking writing of selected words of the system fetch data into said random access memory.

25 27. (Amended) The cache memory apparatus as recited in Claim 22 further comprising:

a miss address register coupled to said host port and to said random access memory for storing a[n] cache miss address signal, the cache miss address signal being selective for [corresponding to a word] words of [said output] the fetch data to be received into said memory update register and corresponding to words of the write back data to be held in said write back register and replaced in said random access memory by the words of fetch data; and

a hit address register coupled to said host port and to said [miss address register] random access memory for storing a[n] cache hit address signal selective for [corresponding to] a word [of said input data] stored in said random access memory.

Please add the following new claim:

26 28. (New) The cache memory apparatus as recited in Claim

further comprising means for identifying ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port, said identifying means being selective for the ones of the fetched data to be provided from said memory update register to said random access memory.

REMARKS

Claims 1, 2, 4-6, and 8-27 are pending in the application. Of those, claims 1, 2, 4-6, 8, 9, 13, 19, and 21-27 have been amended. A new claim 28 has been added.

Responsive to the Examiner's objection to the Abstract of the Disclosure, the Abstract has been amended for clarity and consistency. Responsive to the Examiner's suggestion, the Abstract has been rewritten to include all changes made to date and a copy is enclosed with this response.

The Examiner has required that the label/designation "ads#" within step 300 of Figure 53 be clarified. The label "ads#?" (which was previously amended to include the question mark) identifies the condition evaluated in step 300, namely whether or not the signal ads# has been asserted. The Examiner has also required clarification of the label "assert: brdy# ..." which appears near step 308 in Figure 53. In particular, the Examiner has asked "Does this refer to the cache?" Yes, the label which reads:

```
Cache:    trigger burst read
          assert brdy# to CPU,
          HPOEA#, HPOEB# to burst RAM
          update LRU state
```

identifies actions performed by the cache. Applicant believes the preceding explanations are responsive to the Examiner's

requirement for clarification by way of explanation. Responsive to the Examiner's suggestion, a complete set of the drawings as amended to date (the amendments being highlighted) is enclosed with this response.

Responsive to the Examiner's objection to informalities in the specification, the specification has been amended to correct the errors set forth by the Examiner.

Claims 13 and 27 stand rejected under 35 U.S.C. § 112, second paragraph. The examiner has stated that, in claim 13, it is "unclear how simply 'validating data' itself prevents the writing of data into RAM." Claim 13 has been amended to more clearly claim "means for identifying ones of the fetched data ...." Support for the amendment appears in the Specification at page 53, lines 6-22, and at page 88, line 24, through page 89, line 12. The Examiner's rejection of claim 27 for lack of clarity in antecedent basis has been addressed by more clearly referring to "fetch data." In addition, claim 27 has been amended to more clearly describe cache miss and cache hit address signals and operations. Support for the amendment appears in the Specification at page 16, line 16, through page 17, line 11, and in Table I (pages 28, 39, and 42 -- descriptions of signals WBSTB, QWR, and MWB). Withdrawal of the § 112 rejections is requested.

Summary of the Claimed Invention

The present invention relates to providing a cache memory system which decouples a main memory subsystem from a host data bus. More specifically, the present invention, as set forth in independent claim 1, relates to a cache memory which includes a random access memory (RAM), a host port, a system port, a

memory write register coupled between the host port, the RAM, and the system port, and a write back register coupled between the system port and the RAM. The memory write register buffers data received from the host port and selectively provides the data to the RAM, the system port, or both. The write back register receives data from the RAM and selectively provides the data to the system port. By selectively providing the data to and from the RAM, it is possible to effectively decouple memory accesses at the host port from those at the system port.

Independent claim 4 is of similar scope but adds the further limitation that input data is provided to the RAM from the memory write register at the same time that output data is provided by the write back register to the system port.

Independent claim 19 is of similar scope, relating to a cache memory which includes a RAM, a host port, a system port, a memory write register coupled between the host port and the RAM, and a write back register coupled between the system port and the RAM, but adds the further limitations of a memory update register coupled between the RAM and the system port, and a read hold register coupled between the RAM and the host port. Claim 19 also adds the further limitation that the memory update register holds second input data and selectively provides such data to the RAM. The read hold register provides second output data to the host port at the same time that the memory update register provides second input data to the RAM. By holding and selectively furnishing first output data and holding and selectively providing second input data it is possible to effectively decouple write back and memory update operations at the system port from the RAM.

Finally, independent claim 24 is of similar scope to

claims 1 and 4, but adds the further limitations of a bypass path coupled between the host port and the system port for directly passing data between the host port and the system port, a memory update register coupled between the RAM and the system port, and a read hold register coupled between the RAM and the host port. The memory update register holds system fetch data and selectively provides such data to the RAM. The read hold register allows burst read data to be provided to the host port at the same time that system fetch data is provided to the RAM from the memory update register. By holding and selectively furnishing write back data and holding and selectively providing system fetch data it is possible to effectively decouple write back and memory update operations at the system port from the RAM.

Prior Art Rejections

Claims 1, 2, 4, 6, 8 and 13-15 stand rejected under 35 U.S.C. § 102(b) over Malinowski. Claims 1-27 stand rejected under 35 U.S.C. § 102(e) over Sachs et al. These rejections are traversed in part and in part overcome by amendments to claims 1, 4, 19, and 24. In particular, claims 1, 4, and 24 have been amended to recite the selective provision of data from the memory write register to the RAM, the system port, or both. Basis for these amendments appears in the Specification beginning at page 54, line 17, and continuing through page 55, line 26. In addition, claims 19 and 24 have been amended to recite the selective provision of input data from the memory update register to the RAM, which, together with the holding and selective furnishing of output data from the write back register to the system port, allows memory update and write back operations at the system port to be decoupled from the RAM. Basis for the amendment appears in the Specification at

page 53, lines 6-22, and at page 88, line 24, through page 89, line 12.

In addition, claims 1, 2, 4-6, 8, 9, 13, 19, and 21-27 have been amended to improve clarity by more precisely reciting register limitations (e.g., "write back register") and more clearly reciting function or operation of the registers (e.g., "for holding second data received from said random access memory and selectively providing the second data ..."). Basis for these clarifying amendments appears in the Specification beginning at page 43, line 1, and continuing through page 45, line 23.

Malinowski discloses a memory which includes a memory array and cache registers coupled between the read and write ports of the memory array and input and output ports of the memory. More specifically, Malinowski discloses a first in first out (FIFO) memory array embodiment which includes two pairs of cache registers. One pair, a write pair, is coupled between the data-in port and the memory array write port. The other pair, a read pair, is coupled between the data-out port and the memory array read port. Malinowski also discloses a last in first out (LIFO) memory array embodiment which includes only a single pair of cache registers. One of the cache registers is coupled between the data-in/out port and the read port of the LIFO memory array and the other cache register is coupled between the data-in/out port and the write port of the LIFO memory array. Malinowski sets forth that the technique used for the LIFO memory array could conceivably be used for a random access memory configured with a set of cache registers, a consecutive address generator, and address comparators. *See* Col. 8, lines 16 - 36.

Sachs et al. discloses a cache memory management unit which includes a cache memory subsystem 220 which is coupled to a cache bus via cache output register 230 and cache input register 240 and is coupled to a system bus via system bus input register 260 and system bus output register 250. The cache output register is directly coupled via a data out line to the memory subsystem. The cache input register, system bus input register and system bus output register are coupled to the memory subsystem via a data bus 241.

Neither Malinowski nor Sachs et al., disclose or suggest, taken alone or in combination, a cache memory which includes a memory write register for buffering data received from a host port and selectively providing that data to a RAM, to a system port, or to both, and a write back register for holding data received from the RAM and selectively providing that data to a system port, as required by independent claim 1. Accordingly, amended claim 1 is allowable over Malinowski and Sachs et al. Additionally, neither Malinowski nor Sachs et al., disclose or suggest, taken alone or in combination, the further limitations of a memory update register for holding fetched data and providing the fetched data to the RAM (as required by dependent claim 2), and means for identifying particular fetched data held in the memory update register as not corresponding to write back data held in the write back register, wherein the identifying means is selective for the particular fetched data to be provided from the memory update register to the RAM (as required by dependent claim 13). Accordingly, amended claim 13 (which depends from claim 1 through claim 2) is also allowable over Malinowski and Sachs et al.

Neither Malinowski nor Sachs et al., disclose or suggest, taken alone or in combination, a cache memory which includes a

memory write register for buffering input data received from a host port and selectively providing the input data to a RAM, to a system port, or to both, and a write back register for holding output data received from the RAM and selectively providing the output data to a system port, wherein the input data is provided to the RAM from the memory write register at the same time that the output data is provided by the write back register to the system port, as required by independent claim 4. Accordingly, amended claim 4 is allowable over Malinowski and Sachs et al. Additionally, neither Malinowski nor Sachs et al., disclose or suggest, taken alone or in combination, the further limitations of a miss address register coupled to the host port and to the RAM for storing a cache miss address signal corresponding to a word of write back data to be received from the RAM into the write back register, and a hit address register coupled to the host port and to the RAM for storing a cache hit address signal selective for a word stored in the RAM, as required by dependent claim 5. Accordingly, amended claim 5 is also allowable over Malinowski and Sachs et al.

Neither Malinowski nor Sachs et al., disclose or suggest, taken alone or in combination, a cache memory including a write back register coupled between a RAM and a system port for holding and selectively furnishing output data to the system port, and a memory update register coupled between the RAM and the system port for holding and selectively providing input data to the RAM, wherein the holding and selective furnishing of output data and the holding and selective providing of input data allow write back and memory update operations at the system port to be decoupled from the RAM, as required by independent claim 19. Accordingly, amended claim 19 is allowable over Malinowski and Sachs et al.

Neither Malinowski nor Sachs et al., disclose or suggest, taken alone or in combination, a bypass path coupled between a host port and a system port, a memory write register for buffering and selectively providing memory write data to RAM, to the system port via the bypass path, or to both, a write back register for holding and selectively furnishing write back data to the system port, and a memory update register for holding and selectively providing system fetch data to the RAM, as required by independent claim 24. Accordingly, amended claim 24 is allowable over Malinowski and Sachs et al. Additionally, neither Malinowski nor Sachs et al., disclose or suggest, taken alone or in combination, the further limitations of a miss address register coupled to the host port and to the RAM for storing a cache miss address signal selective for words of fetch data to be received into the memory update register and corresponding to a word of write back data to be held in the write back register and replaced in the RAM by the selected words of fetch data, and a hit address register coupled to the host port and to the RAM for storing a cache hit address signal selective for a word stored in the RAM, as required by dependent claim 27. Accordingly, amended claim 27 is allowable over Malinowski and Sachs et al. Finally, neither Malinowski nor Sachs et al., disclose or suggest, taken alone or in combination, the further limitation of means for identifying particular fetched data held in the memory update register as not corresponding to write back data held in the write back register, wherein the identifying means is selective for the particular fetched data to be provided from the memory update register to the RAM, as required by dependent claim 28. Accordingly, new claim 28 is also allowable over Malinowski and Sachs et al.

Claims 2, 6, 8-10, and 13-18 depend from claim 1 and are

allowable with it. Claims 5, 11, and 12 depend from claim 4 and are allowable with it. Claims 20-23 depend from claim 19 and are allowable with it. Finally, claims 25-28 depend from claim 24 and are allowable with it.

In summary, the Abstract and Specification have been amended to address the Examiner's objections. The Examiner's objections to the Drawings have been addressed by way of explanation. Additionally, the Examiner's §§ 112, 102(b), and 102(e) rejections have been overcome by amendments.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

Respectfully submitted,

Stephen A. Terrile
Attorney for Applicant(s)
Reg. No. 32,946

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on 4/24 1995

4/24/95
Date of Signature

Attorney for Applicant

EXHIBIT 16

07/678,914

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/678,914	04/01/91	CHAN A	M-1018-2P-US

EXAMINER
ELMORE, R

ART UNIT	PAPER NUMBER
2312	5

DATE MAILED: 01/14/93

B. NOEL KIVLIN
SKJERVEN, MORRILL, MACPHERSON,
FRANKLIN & FRIEL
25 METRO DRIVE, SUITE 700
SAN JOSE, CA 95110

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire _____ month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☒ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 1-14 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-14 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

1. Claims 1-14 are presented for examination.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

3. The letter filed 3-16-92 concerning small entity status has been entered into the file. Applicant is referred to MPEP 509.03, pages 500-516, column 2, paragraph 2 et seq.

4. The Abstract of the Disclosure is objected to because the abstract can not contain more than one paragraph.

Applicant is reminded of the proper language and format of an Abstract of the Disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 250 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said", should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Correction is required. See M.P.E.P. § 608.01(b).

5. The disclosure is objected to because of the following informalities:

(a) It is noted that although the present application does contain line numbers in the specification and claims, the line numbers in the claims do not correspond to the preferred format. It is suggested that every fifth line of every claim be numbered, with each new claim beginning with line 1. For ease of reference by both the examiner and applicant all future correspondence should include the recommended line numbering.

Appropriate correction is required.

6. Claim 1-14 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are indefinite because:

(a) It is unclear as to where the plurality of cache addresses are stored and as to how a comparison is achieved in claim 1.

(b) It is unclear as to what is meant by "replaced data" in claims 1 and 2.

(c) It is unclear as to what is actually occuring in the step of "providing said replaced data to said system port" because making the data available to a port does not appear to be a constructive step. In fact, the step which recites "is provided" appear to be unclear and indistinct in that "providing" or "making available" does not constitute an action because the data is not transferred or used in any way, it is only present. A step in a method claim which does not perform an action is indefinite in nature. This rejection applies method claims 1-3 and 12-13.

(d) "the same time" lacks clear antecedent basis -- claim 5;

(e) It is unclear in claim 10 as to why data must be loaded from a peripheral device when the claim states there is a hit condition in the dual port cache memory.

(f) "the further step" lacks clear antecedent basis -- claim 13.

7. The following is a quotation of the appropriate paragraphs

of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-8 and 11-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Thomas et al.

Thomas teaches the invention (claim 4) as claimed, including a computer system comprising:

(a) a processor (e.g., see Figure 1);

(b) a system memory (e.g., see Figure 1);

(c) a dual port cache (e.g., see Figure 1); and,

(d) a cache controller (e.g., see Figure 1).

As to claim 5, Thomas teaches providing an address to the move out queue which is different from the address requested by the processor (e.g., see col. 5, lines 40 et seq.).

As to claim 6, Thomas teaches data can be transferred on the host bus asynchronously to data transferred on the system bus (e.g., see col. 5, lines 40 et seq.).

As to claim 7, Thomas teaches controlling the addressing sequence for the system memory on the system bus and controlling the addressing sequence for the processor on the host bus (e.g., see col. 5, lines 40 et seq.).

As to claim 8, Thomas teaches the system bus does not need to be accessed for a cache hit condition but that this is a local bus access request (e.g., see col. 2, lines 50 et seq.).

As to claim 11, Thomas teaches system memory operates at a different frequency that the processor (e.g., see col. 1, lines 18 et seq.).

As to claim 12, Thomas teaches when data is provided from system memory for a processor request, the data is sent directly to the processor (e.g., see col. 4, lines 32-55).

Method claims 1-3 and 13-14 do not teach or define over the above rejected apparatus claims and are rejected on the same basis.

9. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

10. Claims 9 and 10 are rejected under 35 USC § 103 as being unpatentable over Thomas et al.

Claims 9 and 10 are directed to peripheral memory devices for storing data which may or may not be needed during the course of processing. It is common practice in the memory arts to use low cost storage, such as disk storage, when this type of processing situation occurs. The use of maintaining part of the data in peripheral storage and moving in blocks of data as the processor requests data only resident on the peripheral storage is well known and official notice is taken thereof.

It would have been obvious to one of ordinary skill in the

art of memory storage at the time the invention was made to utilize disk storage or other peripheral storage to maintain data which the processor may need for processing because large amounts of peripheral storage is more economical to use than trying to maintain all data which may be required in the much more expensive system memory or cache memory and the techniques for using such peripheral storage in a cache system are well documented.

11. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Holland et al. teaches a data processing system having instructive responsive apparatus for both a basic and an extended instruction set.

Ziegler et al. teaches a dual port cache with interleaved read access during alternate half-cycles and simultaneous writing.

Matick et al. teaches a distributed on-chip cache.

Moussouris et al. teaches a CPU chip having a tag comparator and address translation unit on chip and connected to off-chip cache and main memories.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba. I. Elmore whose telephone number is (703) 308-1619.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0754.

Reba I. Elmore
January 5, 1993

JOSEPH L. DIXON
SUPERVISORY PATENT EXAMINER
GROUP 2300

EXHIBIT 17

07/678914

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/678,914	04/01/91	CHAN	A M-1018-2P-US

EXAMINER
ELMORE, R

E3M1/0920

B. NOEL KIVLIN
SKJERVEN, MORRILL, MACPHERSON,
FRANKLIN & FRIEL
25 METRO DRIVE, SUITE 700
SAN JOSE, CA 95110

ART UNIT	PAPER NUMBER
2312	9

DATE MAILED: 09/20/93

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 6-17-93 ☒ This action is made final.

A shortened statutory period for response to this action is set to expire 3 (THREE) month(s), 0 days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☒ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 4-11 & 15-21 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☒ Claims 1-3 and 12-14 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 4-11 and 15-21 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 9-89)

1. Claims 4-11 and 15-21 are presented for examination. Claims 1-3 and 12-14 have been cancelled by the amendment filed 6-17-93.

2. The objection to the title is withdrawn due to the amendment.

3. The objection to the Abstract is withdrawn due to the amendment.

4. The drawings are objected to because:

(a) From the Brief Description of the Drawings, Figures 6 and 7 appear to be prior art and should be so designated. Figures which illustrate prior art should be designated by a legend such as "Prior Art" in order to clarify what is the applicant's invention (see MPEP 608.02(g)).

(b) There is not a Figure 8 in the application. Figures 8A, 8B and 8C have not been described in the Brief Description of the Drawings. All references to Figure 8 in the specification should be corrected.

(c) Suitable meaningful legends, (not ambiguous labels or initials), are required for unlabeled or inadequately labeled drawing elements of Figures 8B and 8C (see 37 CFR 1.84(g)). The subarrays of Figure 8B should be so labeled. Appropriate labels should be shown in Figure 8C also.

Correction is required.

Applicant is reminded of the provisions of MPEP 608.02(q) and 608.02(r) regarding a separate draftsman's letter.

5. The disclosure is objected to because of the following informalities:

(a) Figure 8 is described in the specification, however there is not a Figure 8 provided in the drawings. Appropriate correction is required.

6. The rejections under 35 USC 112, second paragraph, are withdrawn due to the amendment. The following rejection under 35 USC 112, second paragraph, is given due to the amendment.

7. Claim 21 is rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are indefinite because:

(a) "said system input register" lacks clear antecedent basis -- claim 21.

8. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 4-11 and 15-21 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Holland et al.

Holland teaches the invention (claims 4, 15 and 21) as claimed, including a computer system comprising:

(a) a microprocessor (CPU) (e.g., see Figure 1, element 35);

(b) a system memory (e.g., see Figure 1, element 16);

(c) a dual port cache (e.g., see Figure 1, element 17);

(d) a host input register connected to the dual port cache and the host data bus for providing data from the host data bus to the dual port cache (e.g., see Figure 2, element 54);

(e) a system output register connected to the dual port cache and the system data bus for receiving data from the dual port cache memory and providing data to the system memory (e.g., see Figure 2, element 46);

(f) a controller connected to the dual port cache memory and the host address bus is taught as a control processor, the controller compares a host address to the addresses in the dual port cache (e.g., see Col. 7, lines 14-38);

(g) when a cache match results from the address comparing of the controller, data from the input register is placed in the dual port cache (e.g., see col. 11, lines 17 et seq.); and,

(h) data from the system memory is placed in the cache when data requested by the CPU is not present in the cache without overwriting host data (e.g., see col. 11, lines 49 et seq.)..

As to claim 5, Holland teaches the controller is connected to the cache memory and provides a first address on the host address bus concurrently with providing a second address on the system address bus with the first address being different than the second address (e.g., see col. 11, lines 17-36).

As to claim 6, Holland teaches data transferred from the host to the cache is asynchronous to the data transferred from the cache to the system memory (e.g., see col. 11, lines 17-36).

As to claim 7, Holland teaches control sequencing to the extent claimed (e.g., see col. 32, lines 62 et seq.).

As to claim 8, Holland teaches disabling the dual port cache (e.g., see Figure 1, element 39).

AS to claims 9-10, Holland teaches a peripheral device is coupled to the system memory and that the peripheral device can contain data which may be requested by the CPU and which can be transferred to the dual port cache (e.g., see col. 7, lines 36-41).

As to claim 11, Holland inherently teaches the CPU and the memory operate at different speeds as dynamic RAM operates at a slower speed than the CPUs of the systems discussed in the Background of the Invention in columns 1 and 2.

As to claim 16, Holland teaches data can be transferred from the CPU to the input register while data is input to the dual port cache (e.g., see col. 10, lines 32-50).

As to claim 17, Holland teaches a plurality of data locations can be transferred during one clock cycle (e.g., see col. 15, lines 16 et seq.).

As to claim 18, Holland teaches the host port can be coupled to the system port when a read miss occurs (e.g., see Figure 1).

As to claim 19, Holland teaches data is placed in the input register in a first clock cycle and data is transferred to the system memory during a second clock cycle (e.g., see col. 11, lines 17 et seq.).

As to claim 20, Holland teaches the dual port cache

comprises a plurality of random access memories (e.g., see col. 9, lines 49-60).

10. Applicant's arguments with respect to claims 4-10 and 15-21 have been considered but are deemed to be moot in view of the new grounds of rejection.

11. Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL.** See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba..I. Elmore whose telephone number is (703) 305-3819.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Reba I. Elmore

September 18, 1993

JOSEPH L. DIXON
SUPERVISORY PATENT EXAMINER
GROUP 2300

EXHIBIT 18

08/170642

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/170,642	12/20/93	CHAN	A M101133C

EXAMINER
ELMORE, R

B3M1/1218

STEPHEN A. TERRILE
SKJERVEN, MORRILL, MACPHERSON,
FRANKLIN & FRIEL
25 METRO DRIVE, SUITE 700
SAN JOSE, CA 95110

ART UNIT	PAPER NUMBER
2318	17

DATE MAILED: 12/18/95

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on 12-20-93 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☒ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 4-11 & 15-32 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☒ Claims 1-3 & 12-14 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 4-11 & 15-32 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

1. Claims 4-11 and 15-32 are presented for examination.

2. The changes to Figures 8B and 8C are approved by the examiner, however, applicant is reminded of the provisions of MPEP 608.02(q) and 608.02(r) regarding a separate draftsman's letter.

3. Claim 21 is rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim is indefinite because:

(a) "said data bus" lacks proper antecedent basis, a host data bus and a system data bus have been previously claimed, it is not clear which data bus 'said data bus' is referencing -- claim 21, lines 13-14.

4. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

5. Claims 4-11 and 15-21 are rejected under 35 USC § 103 as being unpatentable over Baldwin et al.

Baldwin teaches the invention (claims 4, 15 and 21) substantially as claimed, including a computer system and method for operation a memory cache apparatus, the system and method comprising:

(a) a host microprocessor having a host address bus and a host data bus (e.g., see col. 9, lines 39-52 and Figure 1);

(b) an input register connected to the cache memory and the host data bus (e.g., see col. 50, lines 33-42);

(c) a system memory having a system address bus and a system data bus (e.g., see Figures 34-37, 41);

(d) a tri-port cache memory which essentially functions as a dual port cache memory and connects to a system bus and a host bus (e.g., see col. 15, lines 45-62); and,

(e) an input register connected to the dual port cache memory and the system data bus (e.g., see col. 67, line 47 to col. 70, line 30).

Baldwin does not specifically teach a cache controller connected to the dual port cache memory, however, functions performed by a cache controller are performed by the three processors connected to the data cache memory (e.g., see col. 15, line 17 to col. 16, line 11). It would have been obvious to one of ordinary skill in the art of memory storage at the time the invention was made to equate the functions of the processor modules to the functions of a cache controller because the

processor modules perform the data control and transfer tasks typically performed by a cache controller.

As to claims 5 and 16-17, Baldwin teaches the host processor concurrently processing tasks with access the cache memory with the other processors of the system (e.g., see col. 1, lines 29-52).

As to claim 6, Baldwin teaches the host data bus is asynchronous to the system data bus (e.g., see col. 1, lines 38-41).

As to claim 7, Baldwin teaches control sequencing of addresses and data signals (e.g., see col. 20, line 63 to col. 21, line 51).

As to claim 8, Baldwin teaches local bus cycles (e.g., see col. 15, lines 45-62).

As to claims 9 and 10, Baldwin teaches a peripheral device coupled to the system which provides data to the cache (e.g., see col. 16, lines 25-62).

As to claim 11, Baldwin teaches sub-systems operating at different parameters (e.g., see col. 3, line 27 to col. 6, line 15).

As to claims 18-20, Baldwin teaches data is moved to the cache to and from by the processors during clock cycles (e.g., see col. 15, line 15 to col. 16, line 24).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba. I. Elmore whose telephone number is (703) 305-3819.

The examiner can normally be reached on Monday-Thursday from 6:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tod R. Swann, can be reached on (703) 308-7791. The fax phone number for this Group is (703) 305-9565.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Reba I. Elmore
Primary Examiner
December 8, 1995

EXHIBIT 19

08/170642

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/170,642	12/20/93	CHAN	A M10183C

B3M1/0106

STEPHEN A. TERRILE
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EXAMINER	
ELMORE, R	
ART UNIT	PAPER NUMBER
2318	24

DATE MAILED: 01/06/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 10-17-96

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 4-11 & 15-32 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 4-11 & 15-32 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of Reference Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 23

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

-- SEE OFFICE ACTION ON THE FOLLOWING PAGES --

1. Claims 4-11 and 15-32 are presented for examination.

2. The amendment filed 10-17-96 does not meet requirements for the filing of amendments to the claims under 37 CFR 1.21(b). After the claim number for an amended claim the applicant must state either the claim is amended or the number of times the claim is amended, such as:

Claim 4. (amended) or Claim 4. (twice amended), whichever is applicable.

3. The rejection under 35 USC 112, second paragraph, is maintained since the submitted amendment to claim 21 could not be entered.

4. The rejection under 35 USC 103 is maintained.

5. As to the remarks, Baldwin teaches the present invention to the extent claimed. A cache memory is a fast memory element and without specific caching details appearing in the claims, any memory element, especially one designated by the reference as a cache is considered equivalent to a cache memory unless specific details of the claimed cache are present in the claims. The same is true for a processor which is claimed as a 'host processor.' Without supporting limitations within the body of the claim requiring specifics of a host processor which read over the host processor of the prior art, the limitations are considered taught to the extent claimed.

As to the input registers, the holding registers and output registers are taught to the extent claimed for claims 21 and 22. The rejection cites sections of the reference for claim 22 ans well as the other independent claims.

6. As the applicant amendment could not be entered, this office action will not be made final at this time.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba. I. Elmore whose telephone number is (703) 305-3819.

The examiner can normally be reached on Monday-Thursday from 6:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tod R. Swann, can be reached on (703) 308-7791. The fax phone number for this Group is (703) 305-9565.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Reba I. Elmore
Primary Examiner
January 4, 1997

EXHIBIT 20

L:\M\1018\2P\O\PAMD.BNK

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alfred K. Chan

Assignee: MOS Electronics, Inc.

Title: RANDOM ACCESS CACHE MEMORY CONTROLLER AND SYSTEM

Serial No.: 07/678,914 Filed: April 1, 1991

Examiner: Group Art Unit: 233

Attorney Docket No.: M-1018-2P US

San Jose, California
October 18, 1991

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application filed April 1, 1991 as follows.

IN THE CLAIMS

Please add Claims 5-14 as follows:

5. (New) The computer system as recited in Claim 4 wherein said cache controller provides a first address on said host address bus at the same time said cache controller provides a second address on said system address bus, said first address corresponding to a different memory location than said second address.

6. (New) The computer system as recited in Claim 1 wherein data on said host data bus is asynchronous to data on said system data bus.

7. (New) The computer system as recited in Claim 1 wherein said cache controller comprises:

a first control sequencer for controlling addressing

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and data signals on said host address bus and on said host data bus; and

a second control sequencer for controlling addressing and data signals on said system address bus and on said system data bus.

5. (New) The computer system as recited in Claim 1 further comprising means for disabling said dual port cache memory during a local bus access cycle.

6. (New) The computer system as recited in Claim 1 further comprising a peripheral device coupled to said system memory.

7. (New) The computer system as recited in Claim 6 wherein said peripheral device provides data to said system data bus, and wherein a hit address memory location within said dual port cache memory is loaded with said data from said peripheral device if the hit address of said dual port cache memory corresponds with an address of said data from said peripheral device.

11. (New) The computer system as recited in Claim 4 wherein said host microprocessor operates at a first frequency, and wherein said system memory operates at a second frequency that is different from said first frequency.

12. (New) The method for operating a cache memory apparatus as recited in Claim 1 further comprising the step of coupling said host port to said system port when a read miss cycle occurs.

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13. (New) The method for operating a memory cache apparatus as recited in Claim 1 wherein said cache memory apparatus further comprises an update register for providing data from said system port to said random access memory, said method comprising the further step of loading update data from said system port into said update register.

14. (New) The method for operating a memory cache apparatus as recited in Claim 1 wherein said step of latching input data into said input register from said host port occurs in a first clock cycle and wherein said step of loading said input data into said random access memory occurs on a second clock cycle, said second clock cycle immediately following said first clock cycle.

REMARKS

Applicant requests the Examiner to add Claims 5-14 as indicated above. Examination and allowance of the pending claims is requested.

Respectfully submitted,

B. Noël Kivlin
Agent for Applicant
Reg. No. 33,929

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on 10-18 1991

10-16-91 Date of Signature

Agent for Applicant

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EXHIBIT 21

9230 #8/B WL 7/14/93

L:\DMS\5855\M 1018-2\00630 9.WP
930614 (spw)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alfred Chan

Assignee: MOS Electronics Corporation

Title: "RANDOM ACCESS CACHE MEMORY CONTROLLER AND SYSTEM"

Serial No.: 07/678,914 Filed: 04/01/91

Examiner: Elmore, R. Group Art Unit: 2312

Attorney Docket No.: M-1018-2P US

San Jose, California
June 14, 1993

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

AMENDMENT

Sir:

Applicant submits the following amendments and remarks in response to the Office Action dated January 14, 1993 in the above-cited case.

IN THE TITLE

Please amend the title of the invention to read:

B1

"CONTROLLER FOR A RANDOM ACCESS DUAL-PORT CACHE MEMORY SYSTEM".

IN THE ABSTRACT

Please amend the abstract as follows:

Please delete numbered lines 20 through 29 of page 121.

IN THE SPECIFICATION

Please amend the specification as follows:

Page 17, line 18, rewrite "ndata" as --data--.

IN THE CLAIMS

Please cancel claims 1-3, and 12-14 without prejudice.

Please amend the claims as follows:

B

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4. (Amended) A computer system comprising:

a host microprocessor having a host address bus and a host data bus;

a system memory having a system address bus and a system data bus;

a dual port cache memory having a system port connected to said system data bus [and], a host port connected to said host data bus, said dual port memory comprising a random access memory and a plurality of registers connecting said random access memory to said host port and said system port, wherein a data path between said host data bus and said system data bus is decoupled by said random access memory and said plurality of registers; and

a cache controller connected to said cache memory, said cache controller having a first port connected to said host address bus and a second port connected to said system address bus.

5. The computer system as recited in Claim 4 wherein said cache controller is connected to said cache memory for providing [provides] a first address on said host address bus [at the] concurrently with providing [same time said cache controller provides] a second address on said system address bus, said first address corresponding to a different memory location than said second address.

Please add the following new claims:

15. (New) A method for operating a memory cache apparatus, said memory cache apparatus including a random access memory, a host port, a system port, a host input register connected to said host port, a system input register connected to said system port, and a system output register

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connected to said system port, said method comprising the steps of:

receiving an address from a host;

comparing said received address to a plurality of addresses stored in said random access memory;

placing a line of cache data from a location in said random access memory into said system output register;

placing data from said host into said host input register;

wherein if said received address does not match one of said plurality of cache addresses:

placing said host data into said location in said random access memory from said host input register;

retrieving system data corresponding to said received address from said system port into said system input register; and

placing said system data corresponding to said received address from said system input register into said location in said random access memory, subsequent to said step of placing said host data into said random access memory, without overwriting said host data.

16. (New) The method for operating a cache memory apparatus as recited in claim 15, further comprising the step of placing subsequent host data into said host input register concurrently with said step of placing a line of cache data.

17. (New) The method for operating a cache memory apparatus as recited in claim 15, wherein data from a plurality of data locations of said random access memory are placed in said system output register during a single clock cycle.

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18. (New) The method for operating a cache memory apparatus as recited in claim 15, further comprising the step of coupling said host port to said system port when a read miss cycle occurs.

19. (New) The method for operating a memory cache apparatus as recited in claim 15, wherein said step of placing data from said host into said host input register occurs in a first clock cycle, and wherein said step of placing said host data into said location in said random access memory occurs on a second clock cycle, said second clock cycle immediately following said first clock cycle.

20. (New) A computer system according to claim 4 wherein said dual port cache memory comprises a plurality of burst random access memories.

21. (New) A computer system comprising:

a host microprocessor having a host address bus and a host data bus for providing a host address and host data;

a system memory for storing system data, said system memory having a system data bus for providing system data;

a dual port cache memory for storing said host data and system data;

a host input register connected to said dual port cache memory and said host data bus for providing data from said host data bus to said dual port cache memory;

a system output register connected to said dual port cache memory and said system data bus for receiving a line of cache data from said dual port cache memory and providing said line of cache data to said system data bus;

a controller connected to said dual port cache memory and said host address bus, said controller containing a

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plurality of addresses for receiving said host address from said host address bus and comparing said host address to said plurality of addresses;

wherein when a match results from said comparing:

host data from said host input register is placed into said dual port cache memory at a location of said line of cache data; and

system data from said system input register is placed into said location of said line of cache data after said host data is placed into said dual port cache memory, wherein said host data is not overwritten.

B21 Cont.

REMARKS

These remarks are in response to the Office Action dated January 14, 1993, which has a shortened statutory period set to expire April 14, 1993. A two-month extension, to expire June 14, 1993, is requested in a petition filed herewith.

Claims 1-14 are pending and rejected under 35 U.S.C. § 112 and over prior art. Claims 4, and 5 are amended. Claims 1-3 are rewritten for clarity. Claims 15-21 are added. Claims 1-3, and 12-14 are canceled. Reconsideration is requested.

The specification is amended for clarity.

The Examiner has objected to the title of the invention. This rejection is overcome by the above amendment to the title.

The Examiner has objected to the abstract. Applicant has amended the abstract to overcome this rejection.

The Examiner has objected to the disclosure for the reason that the claims are not presented in a "preferred format". Applicant traverses the objection on the grounds that (1) line numbering for the claims have been presented in the conventional page line numbering format; and (2) no requirement as made by the Examiner is known in the PTO rules.

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With regard to small entity status, the Assignee's attorneys have reviewed M.P.E.P. § 509.03 and withdraw the request for a determination by the Office on this issue. The facts stated in the letter dated March 10, 1992 in this case are, however, before the Office, and if the Office has any reason to believe that at the time of filing this case was not entitled to small entity status, the Office should so inform Applicant.

Rejections under 35 U.S.C. § 112

Claims 1-14 were rejected under 35 U.S.C. § 112, second paragraph. The Examiner has written:

> It is unclear as to where the plurality of cache addresses are stored and as to how a comparison is achieved in claim 1.

Claim 1 is rewritten for clarity as new claim 15, which recites "...a plurality of addresses stored in said random access memory;...", as supported in the specification on page 12, lines 2-10, and generally throughout. Address comparison techniques are well known in the art of cache memory management. See, e.g., Intel Corporation, "i486 Microprocessor Hardware Manual", pp. 6-1 - 6-11, 1990, a copy of which is submitted in an accompanying Information Disclosure Statement. Applicant need not recite this process in a claim, since it is not believed essential to novelty. See M.P.E.P. 706.03(f).

New claim 15 overcomes the Examiner's rejections to claim 1 under 35 U.S.C. § 112.

The Examiner writes:

> It is unclear as to what is actually occurring in the step of "providing said replaced data to said system port" because making the data available to a port does not appear to be a constructive step... This rejection applies to method claims 1-3 and 12-13.

This rejection is overcome by the new claims. Applicant maintains that "providing data" is a constructive step in that it enables subsequent functions to occur which are conditional

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on the presence of the data.

Claim 5 has been amended for clarity and overcomes the Examiner's rejection thereto under 35 U.S.C. § 112.

The Examiner writes:

> It is unclear in claim 10 as to why data must be loaded from a peripheral device when the claim states there is a hit condition in the dual port cache memory.

As supported in the specification, pages 104 to 106, hits in the cache memory may also be registered by devices other than the CPU. System memory data which has been manipulated by other devices must update the cache, so that the CPU has access to the most recent copy of data. This rejection is therefore respectfully traversed.

Claim 13 is canceled, thereby obviating the Examiner's rejections thereto.

For the above reasons, Applicant requests reconsideration and withdrawal of the rejections under 35 U.S.C. § 112.

Prior Art Rejections

The Examiner rejected claims 1-8 and 11-14 under 35 U.S.C. § 102(b) as being anticipated by Thomas et al. The Examiner writes:

> Thomas teaches the invention (claim 4) as claimed, including a computer system comprising:
> (a) a processor (e.g., see Figure 1);
> (b) a system memory (e.g., see Figure 1);
> (c) a dual port cache (e.g., see Figure 1);
> (d) a cache controller (e.g., see Figure 1);

Figure 1 of Thomas et al. shows an output bus 25 from cache 15 coupled to CPU data bus 38. Bus 25 supplies cache hits to CPU 12. Bus 38 returns move-in data from mainstore memory unit 18. In the event of read hits following a miss, move-in data along bus 38 will contend with CPU reads of the cache along bus 25. Data from both buses cannot traverse one line to the CPU simultaneously since the data paths are coupled. Therefore, cache read hit processing cannot occur

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during the cache update required by the previous miss.

In contrast, claim 4 as amended recites:

> ...said dual port memory comprising a random access memory and a plurality of registers connecting said random access memory to said host port and said system port, wherein a data path between said host data bus and said system data bus is decoupled by said random access memory and said plurality of registers... (Emphasis added).

Support for claim 4 is shown in Applicant's Figure 8 (elements 106, 108, 114A-D, 116A-D, 118A-D, 112 and 113). The specification teaches decoupling of host and system data buses on page 6, lines 20-25, page 115, beginning at line 31 through page 116, line 5. Thomas et al. does not disclose or suggest the structure recited in claim 4.

The structure of claim 4 advantageously provides faster execution by enabling system fetch completion during subsequent CPU read and write cycles, as disclosed on page 61 of the specification, lines 22-34, with reference to Figure 24. Claim 4 therefore distinguishes over Thomas et al.

The Examiner writes:

> Method claims 1-3 and 13-14 do not teach or define over the above rejected apparatus claims and are rejected on the same basis.

Thomas et al. does not disclose transfer of memory between a CPU, a cache memory and a system memory such as would occur during a write miss operation. A write miss operation requiring cache update in the system of Thomas et al. requires either: a CPU write to system memory before moving-in the data from the requested write address, or that the CPU wait until the requested data is moved-in from mainstore memory to the cache memory before updating the cache. In either case, a slow mainstore access is required before the CPU can continue execution, undesirably slowing performance.

Therefore, in contrast to Thomas et al., new claim 15 (replacing claim 1) recites:

> ... placing said system data corresponding to said received address from said system input register into

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said location in said random access memory subsequent to said step of placing said host data into said random access memory without overwriting said host data... (Emphasis added).

Support for new claim 15 is found at page 58 of Applicant's specification, lines 5-12. The method of new claim 15 advantageously provides a faster write miss operation by allowing the CPU to write to the cache immediately and resume execution without waiting for system data to update the cache line. The placing step as recited in new claim 15 is not disclosed or suggested in Thomas et al.

Thomas et al. does not disclose any details of cache updating. Thus move-in operations in Thomas et al. will apparently overwrite all previously written cache data at a cache location, and hence claim 15 distinguishes thereover for the additional reason that claim 15 recites "without overwriting".

Claim 15 therefore distinguishes over Thomas et al. for at least the reasons stated above.

Rejections under 35 U.S.C. § 103

Claims 9 and 10 are rejected under 35 U.S.C. § 103 as being unpatentable over Thomas et al.

Insofar as claim 4 is distinguished over Thomas et al., claims 9 and 10 are likewise distinguished by at least their dependence from claim 4.

Applicant requests reconsideration and withdrawal of the rejections under 35 U.S.C. § 103.

Claims 2, 3, 12 and 14 have been canceled and rewritten for clarity as new claims 16, 17, 18 and 19, which respectively recite the limitations of originally filed claims 2, 3, 12 and 14. No new matter is added.

New claim 20 is supported at page 12 of the specification,

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lines 2-5. The use of burst RAMs in a cache memory reduces the number of clock cycles required to update a cache line, thereby increasing system performance. Thomas et al. does not disclose the structure of new claim 20, and so claim 20 distinguishes over Thomas et al.

New apparatus claim 21 recites many of the same limitations as does new method claim 15, as well as additional structural limitations.

Claim 21 specifically recites:

> ... a host input register connected to said dual port cache memory and said host data bus for providing data from said host data bus to said dual port cache memory;
> a system output register connected to said dual port cache memory and said system data bus for receiving a line of cache data from said dual port cache memory and providing said line of cache data to said system data bus; (Emphasis added).

New claim 21 distinguishes over Thomas et al. for at least the reasons stated above pertaining to claim 4, because claim 21 further recites:

> ... wherein when a hit condition results from said comparison:...system data from said system input register is placed into said location of said line of cache data after said host data is placed into said dual port cache memory wherein said host data is not overwritten. (Emphasis added.)

Therefore new claim 21 distinguishes over Thomas et al. for at least the reasons stated above in support of claim 15.

For the foregoing reasons, independent claims 4, 15 and 21 are deemed allowable. Claims 5-11 and 15-20 are deemed allowable for at least the reason of their dependence from allowable claims 4 and 15.

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Should the Examiner undertake any action other than the allowance of claims 4-11 and 15-21, the Examiner is requested to contact Applicant's attorney at (408) 283-1222.

Respectfully submitted,

Norman R. Klivans

Norman R. Klivans
Attorney for Applicant
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on June 14 1993

June 14, 1993 Norman R. Klivans
Date of Signature Attorney for Applicant

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EXHIBIT 22

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alfred Chan

Assignee: MOS Electronics

Title: RANDOM ACCESS CACHE MEMORY CONTROLLER AND SYSTEM

Serial No: Unknown Filed: 12-20-93

Examiner: Unknown Group Art Unit: Unknown

Attorney Docket No: M-1018-3C

San Jose, California
December 20, 1993

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C.

PRELIMINARY AMENDMENT

Dear Sir:

Kindly preliminarily amend the above-identified application, which is a file wrapper continuation of U.S.S.N. 07/678,914, as follows.

In the Specification:

On page 8, line 6, please add --in accordance with the present invention-- after "system".

On page 8, line 8, please add --in accordance with the present invention-- after "system".

On page 8, line 10, please change "Figure 8 is" to --Figures 8A, 8B and 8C, which are generally referred to as Figure 8 throughout the specification, are--

File History Report

☐ Paper number _____ is missing from the United States Patent and Trademark Office's original copy of the file history. No additional information is available.

☒ The following page(s) 2 of paper number _____ is/are missing from the United States Patent and Trademark Office's original copy of the file history. No additional information is available

Additional comments: _____

In the Drawings:

Please amend the drawings as shown in red on the attached sheets.

In the Claims:

Please amend claims 4 and 21 as follows:

4. (Twice-Amended) A computer system comprising:
a host microprocessor having a host address bus and a host data bus;
a system memory having a system address bus and a system data bus;
a dual port cache memory having a system port connected to said system data bus, a host port connected to said host data bus, said dual port memory comprising a random access memory and a plurality of registers connecting said random access memory to said host port and said system port, wherein a data path between said host data bus and said system data bus is decoupled by said random access memory and said plurality of registers so as to allow concurrent transfer of data to and from said memory cache; and
a cache controller connected to said cache memory, said cache controller having a first port connected to said host address bus and a second port connected to said system address bus such that said cache memory and said cache controller are connected in parallel between said host microprocessor and said system memory.

21. (Amended) A computer system comprising:

a host microprocessor having a host address bus and a host data bus for providing a host address and host data;

a system memory for storing system data, said system memory having a system data bus for providing system data;

a dual port cache memory for storing said host data and system data;

a host input register connected to said dual port cache memory and said host data bus for providing data from said host data bus to said dual port cache memory;

a system [output] input register connected to said dual port cache memory and said system data bus for receiving a line of cache data from said [dual port cache memory] data bus and providing said line of cache data to said [system data bus] dual port cache memory;

a controller connected to said dual port cache memory and said host address bus, said controller containing a plurality of addresses for receiving said host address from said host address bus and comparing said host address to said plurality of addresses;

wherein when a match results from said comparing:

host data from said host input register is placed into said dual port cache memory at a location of said line of cache data; and,

system data from said system input register is placed into said location of said line of cache data after said host data is placed into said dual port cache memory, wherein said host data is not overwritten.

Please add the following new claims:

---

16 ~~22~~. (New) A computer system comprising:

3 Sub F6

a host microprocessor having a host address bus and a host data bus;

a system memory having a system address bus and a system data bus;

a dual port cache memory including

a random access memory,

a host port coupled to the host data bus,

a system port coupled to the system data bus,

a first input register for selectively writing input data to said random access memory, said first input register being coupled between said host port and said random access memory,

a first output register for selectively furnishing output data to said system port, said first output register being coupled between said random access memory and said system port, said input data being provided to said random access memory from said first input register at the same time that said output data is provided by said first output register to said system port,

a second input register for providing second input data to said random access memory, said second input register being coupled between said random access memory and said system port, and

a second output register coupled between said random access memory and said host port for providing second output data from said random access memory to said host port, said second input data being provided to said random access memory from said second input register at the same time that said second output data is provided by said second output register to said system port; and

a cache controller connected to said cache memory, said cache controller having a first port connected to said host address bus and a second port connected to said system address bus such that said cache memory and said cache controller are connected in parallel between said host microprocessor and said system memory,

said cache controller being connected to said cache memory for providing a first address on said host address bus concurrently with providing a second address on said system address bus, said first address corresponding to a different memory location than said second address.

23. (New) The computer system as recited in Claim 22 wherein data on said host data bus is asynchronous to data on said system data bus.

24. (New) The computer system as recited in Claim 22 wherein said cache controller comprises:

a first control sequencer for controlling addressing and data signals on said host address bus and on said host data bus; and

a second control sequencer for controlling addressing and data signals on said system address bus and on said system data bus.

25. (New) The computer system as recited in Claim 22 further comprising means for disabling said dual port cache memory during a local bus access cycle.

26. (New) The computer system as recited in Claim 22 further comprising a peripheral device coupled to said system memory.

27. (New) The computer system as recited in Claim 26 wherein said peripheral device provides data to said system data bus, and wherein a hit address memory location within said dual port cache memory is loaded with said data from said peripheral device if the hit address of said dual port cache memory corresponds with an address of said data from said peripheral device.

28. (New) The computer system as recited in Claim 22 wherein said host microprocessor operates at a first frequency, and wherein said system memory operates at a second frequency that is different from said first frequency.

29. (New) An apparatus as recited in claim 22 further comprising a bypass path coupled between said host port and said system port for directly allowing passage of data between said host port and said system port.

30. (New) An apparatus as recited in Claim 22, wherein said first input register is a memory write register, said second input register is an update register, said first output register is a write back register, and said second output register is a read hold register.

31. (New) The cache memory apparatus as recited in Claim 22 wherein said second input register can store a plurality of words of data.

32. (New) The cache memory apparatus as recited in Claim 31 further comprising means for masking writing of selected words of data into said random access memory.

REMARKS

The above-identified application is a file wrapper continuation of an application which was finally rejected in an Office Action mailed on September 20, 1993. This Preliminary Amendment addresses the issues raised in that final rejection.

The parent application was objected to based upon an objection to the Drawings. Regarding the Examiner's comment about Figures 6 and 7, the description of these figures in the Brief Description of the Drawings has been amended to clearly set forth that these drawings are not prior art but rather block diagrams of computer systems which include a cache memory in accordance with the present invention. Additionally, the description of Figures 8A, 8B and 8C has been amended to clearly set forth that the combination of all of these figures is generally referred to as Figure 8. The legends and subarrays of Figures 8B and 8C have been amended to correct the errors set forth by the Examiner.

The parent application was objected to based upon an objection to the Specification. Responsive to this objection to the Specification, the Specification has been amended. No new matter has been added.

Claim 21 of the parent application was rejected under 35 U.S.C. §112, second paragraph. Claim 21 has been amended to address this rejection.

Independent claims 4, 15, and 21 of the parent application were rejected under 35 U.S.C. §102 over Holland et al. This rejection is respectfully traversed.

The present invention relates to a computer system which includes a cache memory system and a cache controller which decouple a main memory subsystem from a host data bus. More specifically, the present invention, as set forth in independent claim 4, relates to a computer system which includes a host microprocessor, a system memory, a dual port cache memory and a cache controller. The cache memory includes a random access memory, a host port, a system port, and a plurality of registers connecting the random access memory to the host port and the system port. The plurality of registers allow the host data bus to be decoupled from the system address bus, thus allowing concurrent transfer of data to and from the memory cache. The cache controller and the cache memory are connected in parallel between the host microprocessor and the system memory, thus allowing the host microprocessor to be decoupled from the system memory. Independent claim 21 is of similar scope to independent claim 4 but specifies a host input register connected to the dual port cache memory and the host data bus for providing data from the host data bus to the dual port cache memory, a system input register connected to the dual port cache memory and the system data bus for receiving a line of cache data from the data bus and providing the line of cache data to the dual port cache memory, and a controller which contains a plurality of addresses for receiving the host address from the host address bus and comparing the host address to the plurality of addresses. When a match results from the comparing, host data from the host input register is placed into the dual port cache memory at a location of the line of cache data and system data from the system input register is placed into the location of the line of cache data after the host data is placed into the dual port cache memory such that the host data is not overwritten. Independent claim 15 is a method claim of similar scope to independent claim 21.

The present invention, as set forth by new independent claim 22, relates to a computer system which includes a host microprocessor, a system memory, a dual port cache memory and a cache controller. The cache memory includes a random access memory, a host port, a system port, a first and second input registers and first and second output registers. The first input register is coupled between the host port and the random access memory and selectively writes input data to the random access memory. The first output register is coupled between the random access memory and the system port and selectively furnishes output data to the system port. The input data is provided to the random access memory from the first input register at the same time that the output data is provided by the first output register to the system port. The second input register is coupled between the random access memory and the system port and provides second input data to the random access memory. The second output register is coupled between the random access memory and the host port and provides second output data from the random access memory to the host port. The second input data is provided to the random access memory from the second input register at the same time that the second output data is provided by the second output register to the system port. The cache controller is connected to the cache memory and has a first port connected to the host address bus and a second port connected to the system address bus such that the cache memory and the cache controller are connected in parallel between the host microprocessor and the system memory. The cache controller provides a first address on the host address bus to the cache memory concurrently with providing a second address on the system address bus; the first address corresponds to a different memory location than the second address.

Holland et al. discloses a data processing system which includes a system memory, a bank controller, a system cache, a microprocessor portion and an I/O portion. The memory bank controller provides an interface between the system cache and the main memory unit. The interface between the system memory and the remainder of the system is via the dual port system cache. The system memory is coupled to the bank controller which is coupled to a memory system port of the system cache. The system cache also includes a CPU requestor port, via which the system cache services requests from the microprocessor portion, and an I/O requestor port, via which the system cache services requests from the I/O portion.

The system cache of Holland et al. includes a cache store array which is coupled to a plurality of registers which are coupled to respective ports; the system cache also includes a direct access path between the I/O port and the memory system port. The system cache uses the various registers to provide pipelining operations so that accesses to one of the input ports may be intertwined with accesses to the other input port. The system cache also may perform direct write transfers between the input ports and the main memory using a block write transfer. During a block write transfer, the data is written directly into the main memory via data write register 40A, multiplexer 48 ånd write data register 46.

Holland et al. does not disclose or suggest providing memory cache with a plurality of registers to allow a host data bus to be decoupled from a system address bus, thus allowing concurrent transfer of data to and from the memory cache or connecting a cache controller and a cache memory in parallel between a host microprocessor and a system memory, thus allowing the host microprocessor to be decoupled from the system memory, all as

required by independent claim 4. Additionally, Holland et al. does not disclose or suggest a host input register connected to the dual port cache memory and the host data bus for providing data from the host data bus to the dual port cache memory, a system input register connected to the dual port cache memory and the system data bus for receiving a line of cache data from the data bus and providing the line of cache data to the dual port cache memory, as required by independent claims 15 and 21. Additionally, Holland et al. does not disclose or suggest a cache memory which includes a first input register which is coupled between a host port and a random access memory and selectively writes input data to the random access memory, a first output register which is coupled between the random access memory and a system port and selectively furnishes output data to the system port, a second input register which provides second input data to the random access memory and is coupled between the random access memory and the system port, and a second output register which provides second output data to the host port and is coupled between the random access memory and the host port, as required by new independent claim 22. Accordingly, Holland et al. could not disclose a computer system which includes a cache memory in which input data is provided to the random access memory from the first input register at the same time that the output data is provided by the first output register to the system port and second input data is provided to the random access memory from the second input register at the same time that the second output data is provided by the second output register to the system port, as required by new independent claim 22. Accordingly, independent claims 4, 15 and 21 and new independent claim 22 are allowable over Holland et al.

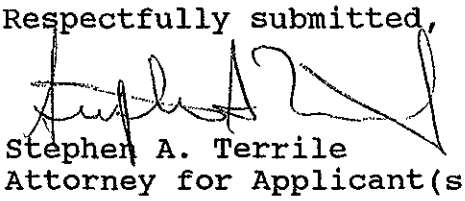
Claims 5 - 11 and 20 depend from independent claim 4 and are allowable for at least this reason. Claims 16 - 19 depend from

independent claim 15 and are allowable for at least this reason. Claims 23 - 32 depend from independent claim 22 and are allowable for at least this reason.

In summary, the Examiner's objection to the Drawings and Specification have been addressed. Additionally, the rejection under 35 U.S.C. §102(b) over Holland et al. has been traversed.

Accordingly, the application is now in condition for allowance, and such allowance is respectfully solicited.

Respectfully submitted,



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Dec. 20, 1993 Teri Alloway
Date of Signature

EXHIBIT 23

PATENT #22E

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Alfred Chan		
Assignee:	MOS Electronics		
Title:	RANDOM ACCESS CACHE MEMORY CONTROLLER AND SYSTEM		
Serial No.:	08/170,642	Filed:	December 20, 1993
Examiner:	Elmore, R.	Group Art Unit:	2318
Atty. Docket No.:	M-1018-3C US		

San Jose, California
October 16, 1996

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

This paper is responsive to the Office action mailed June 18, 1996 having a shortened statutory period set to expire September 18, 1996. Accompanying this response is a petition to extend the shortened statutory period by one (1) month, setting a new time for response of October 18, 1996. Further examination and reconsideration are respectfully requested in view of the amendments and remarks set forth below.

PROVISIONAL PETITIONS

The Office is provisionally petitioned to extend the shortened statutory period as necessary to avoid abandonment of the Application in relation to the outstanding Office action. If appropriate, a separate Petition for Extension accompanies this Response, this provisional petition being effective in the event that the separate Petition for Extension is

defective or missing. The Office is provisionally authorized to charge any amount required to avoid abandonment of the Application in relation to the outstanding Office action to account number 19-2386. A separate Fee Transmittal accompanies this Response, this provisional fee authorization being effective in the event that the separate Fee Transmittal is defective or missing.

↓ Below amendments were not entered as they failed to comply with RL 121(b) see paragraph 2 paper 24

AMENDMENTS

In the Claims

Please amend the claims as follows:

4. A computer system comprising:

a host [microprocessor] processor having a host address bus and a host data bus;

a system memory having storage locations addressable by said host processor, a system address bus and a system data bus;

a dual port cache memory having a system port connected to said system data bus [,] and a host port connected to said host data bus, said dual port cache memory comprising [a random access memory] cache storage locations dynamically associable with said storage locations of said system memory and a plurality of registers [connecting] coupling said [random access memory] cache storage locations to said host port and said system port, wherein a data path between said host data bus and said system data bus is operably decoupled by buffering and selective provision of data to and from said [random access memory and] cache storage locations by said plurality of registers so as to allow concurrent transfer of data to and from said dual port cache memory [cache]; and

a cache controller connected to said dual port cache memory, said cache controller having a first port connected to said host address bus and a second port connected to said system address bus such that said dual port cache

memory and said cache controller are connected in parallel between said host [microprocessor] processor and said system memory.

5. The computer system as recited in Claim 4 wherein said cache controller is connected to said dual port cache memory for providing a first address on said host address bus concurrently with providing a second address on said system address bus, said first address corresponding to a different [memory location] one of said storage locations of said system memory than said second address.

11. The computer system as recited in Claim 4 wherein said host [microprocessor] processor operates at a first frequency, and wherein said system memory operates at a second frequency that is different from said first frequency.

15. A method for operating a memory cache apparatus, said memory cache apparatus including [a random access memory] addressable storage, a host port, a system port, a host input register connected to said host port, a system input register connected to said system port, and a system output register connected to said system port, said method comprising the steps of:

receiving an address from a host;

comparing said received address to a plurality of addresses corresponding to cache data stored in said [random access memory] addressable storage;

placing a line of said cache data from a location in said [random access memory] addressable storage into said system output register;

placing data from said host into said host input register;

wherein if said received address does not match one of said plurality of [cache addresses] addresses corresponding to said cache data:

placing said host data into said location in said [random access memory] addressable storage from said host input register;

receiving system data corresponding to said received address from said system port into said system input register; and

subsequent to said step of placing said host data into said addressable storage, and without overwriting said host data, placing said system data corresponding to said received address from said system input register into said location in said [random access memory,] addressable storage.

[subsequent to said step of placing said host data into said random access memory, without overwriting said host data.]

17. The method for operating a cache memory apparatus as recited in claim 15, wherein data from a plurality of data locations of said [random access memory] addressable storage are placed in said system output register during a single clock cycle.

19. The method for operating a memory cache apparatus as recited in claim 15, wherein said step of placing data from said host into said host input register occurs in a first clock cycle, and wherein said step of placing said host data into said location in said [random access memory] addressable storage occurs on a second clock cycle, said second clock cycle immediately following said first clock cycle.

21. A computer system comprising:

a host [microprocessor] processor having a host address bus and a host data bus for providing a host address and host data;

a system memory for storing system data, said system memory having a system data bus for providing system data;

a dual port cache memory for storing said host data and system data[;] , said dual port cache memory including:

addressable memory storage;

a host input register [connected to said dual port cache memory and] coupled to said addressable memory storage and to said host data bus for providing data from said host data bus to said [dual port cache memory] addressable memory storage; and

a system input register [connected to said dual port cache memory and] coupled to said addressable memory storage and to said system data bus for receiving a line of said cache data from said data bus and providing said line of cache data to said [dual port cache memory] addressable memory storage; and

a controller connected to said dual port cache memory and said host address bus, said controller containing a plurality of addresses corresponding to said cache data for receiving said host address from said host address bus and comparing said host address to said plurality of addresses[;] , wherein when a match results from said comparing:

host data from said host input register is placed into said [dual port cache memory] addressable memory storage at a location of said line of cache data; and

system data from said system input register is placed into said location of said line of cache data after said host data is placed into said [dual port cache memory] addressable memory storage, wherein said host data is not overwritten.

22. A computer system comprising:

a host microprocessor having a host address bus and a host data bus;

a system memory having a system address bus and a system data bus;

a dual port cache memory including:

[a random access memory] addressable storage,

a host port coupled to the host data bus,

a system port coupled to the system data bus,

a first input register for selectively writing input data to said [random access memory] addressable storage, said first input register being coupled between said host port and said [random access memory] addressable storage,

a first output register for selectively furnishing output data to said system port, said first output register being coupled between said [random access memory] addressable storage and said system port, said input data being provided to said [random access memory] addressable storage from said first input register at the same time that said output data is provided by said first output register to said system port;

a second input register for providing second input data to said [random access memory] addressable storage, said second input register being coupled between said [random access memory] addressable storage and said system port, and

a second output register coupled between said [random access memory] addressable storage and said host port for providing second output data from said [random access memory] addressable storage to said host port, said second input data being provided to said [random access memory] addressable storage from said second input register at the same time that said second output data is provided by said second output register to said system port; and

a cache controller connected to said dual port cache memory, said cache controller having a first port connected to said host address bus and a second port connected to said system address bus such that said cache memory and said cache controller are connected in parallel between said host [microprocessor] processor and said system memory,

said cache controller being connected to said dual port cache memory for providing a first address on said host address bus concurrently with providing a second address on said system address bus, said first address corresponding to a different memory location than said second address.

REMARKS

Claim 21 was rejected under 35 U.S.C. § 112, second paragraph. The Examiner stated that "'said data bus' lacks proper antecedent basis." Claim 21 has been amended to provide proper antecedent basis. Further consideration is requested.

The Examiner rejected claims 4, 15, 21, 22, and those dependent therefrom (i.e., 4-11 and 15-32) under 35 U.S.C. § 103 as being unpatentable over United States Patent No. 5,329,630 to Baldwin. In particular, the Examiner writes:

> Baldwin teaches the invention (claims 4, 15 and 21) substantially as claimed, including a computer system and method for operation a memory cache apparatus, the system and method comprising:
>
> (a) a host microprocessor having a host address bus and a host data bus (e.g., see col. 9, lines 39-52 and Figure 1);
>
> (b) an input register connected to the cache memory and the host data bus (e.g., see col. 50, lines 33-42);
>
> (c) a system memory having a system address bus and a system data bus (e.g., see Figures 34-37, 41);
>
> (d) a tri-port cache memory which essentially functions as a dual port cache memory and connects to a system bus and a host bus (e.g., see col. 15, lines 45-62); and,
>
> (e) an input register connected to the dual port cache memory and the system data bus (e.g., see col. 67, line 47 to col. 70, line 30).
>
> Baldwin does not specifically teach a cache controller connected to the dual port cache memory, however, functions performed by a cache controller are performed by the three processors connected to the cache memory (e.g., see col. 15, line 17 to col. 16, line 11). It would have been obvious to one of ordinary skill in the art of memory storage at the time the invention was made to equate the functions of the processor modules to the functions of a cache controller because the processor modules perform the data control and transfer tasks typically performed by a cache controller.

This rejection is traversed. Applicant respectfully suggests that the Examiner's interpretation of Baldwin is not in accordance with the disclosure thereof. Nonetheless, claims 4, 15, 21 and 22 (and those dependent therefrom) have been amended to obtain a more appropriate scope of coverage and to better distinguish over art made of record but not relied upon by the Examiner (e.g., Sachs et al.).

Regarding the art relied upon by the Examiner, Baldwin discloses a double buffering system wherein a dual port memory is partitioned in software so that the top half of the memory is allocated to one processor and the bottom half to the other. The double buffering is implemented by switching the allocation under control of the two processors. *See* Baldwin, Abstract. Baldwin's data cache memory 140 is a cache in name only. In reality, data cache memory 140 is merely a small, wide, fast memory for use in a numeric processing subsystem of a larger computer system. *See* Baldwin, Col. 9, lines 14-37. Data cache memory 140 does not function as a cache providing a processor with high speed access to frequently used memory locations while accesses to uncached locations are serviced by a lower speed memory device. Instead, data cache memory 140 is loaded with data in response to commands from a host processor external to the numeric processing subsystem. *See* Baldwin, Col. 106, line 6 - Col.107, line 66. Both the host processor and system memory reside on a VME-bus (*see* Baldwin, Figs. 34-37, and 41) which couples to the numeric processing subsystem of Fig. 1 via host (or VME) external interface controller 160 (*see* Baldwin, Col. 10, lines 16-30).

Several points are made clear by Baldwin's discussion of his physical memory model in the context of a host processor command to the numeric processing subsystem to multiply two arrays and store the results in a third array, wherein all three arrays reside in VME memory space. First, data cache memory 140 is not a cache in the traditional sense of the term. Second, the "processors" to which data cache is coupled are themselves tightly coupled in their respective numeric, control, and data transfer functions, interrupting each other to gain access to resources including data cache 140. Third, both the host processor and the system memory are external to the numeric processing subsystem, i.e., reside on a VME bus across external (VME) interface 160 from the numeric processing subsystem and "data cache" memory 140. *See* Baldwin, Col. 106, line 6 - Col.107, line 66. In short, data cache memory 140 can not be said to be a cache in the traditional sense, floating point processor is not a host processor initiating loads and stores to addresses in an address space greater than that represented in "data

cache" memory 140, and neither a host processor nor system memory resides on the numeric processor side (i.e., "data cache" side) of the an external VME interface.

United States Patent No. 5,091,846 to Sachs, et al. has been made of record but not relied upon by the Examiner. Applicant wishes the Examiner to consider Sachs et al. in light of the following. Sachs et al. disclose a cache memory management unit which includes a cache memory subsystem 220 which is coupled to a cache bus via cache output register 230 and cache input register 240 and is coupled to a system bus via system bus input register 260 and system bus output register 250. The cache output register is directly coupled via a data out line to the memory subsystem. The cache input register, system bus input register and system bus output register are coupled to the memory subsystem via a data bus 241.

In contrast with both of the above-described references, an embodiment of the present invention, as set forth by amended independent claim 4, relates to a computer system which includes a host processor, a system memory, a dual port cache memory, and a cache controller. The host processor has a host address bus and a host data bus. The system memory has storage locations addressable by the host processor and has a system address bus and a system data bus. The dual port cache memory includes cache storage locations dynamically associable with the storage locations of the system memory, a host port, a system port, and a plurality of registers coupling the cache storage locations to the host port and the system port. The system port is connected to the system data bus and the host port is connected to the host data bus. A data path between the host data bus and the system data bus is operably decoupled by buffering and selective provision of data to and from the cache storage locations by the registers, allowing concurrent transfer of data to and from the dual port cache memory.

Another embodiment of present invention, as set forth by amended independent claim 21, is of similar scope to independent claim 4 but specifies a host input register coupled to the addressable memory storage of the dual port cache memory and to the host data bus for providing data from the host data bus to the addressable memory storage, a

system input register coupled to the addressable memory storage and to the system data bus for receiving a line of cache data from the data bus and providing the line of the cache data to the addressable memory storage, and a controller which contains a plurality of addresses corresponding to the cache data for receiving the host address from the host address bus and comparing the host address to the plurality of addresses. When a match results from the comparing, host data from the host input register is placed into the addressable memory storage at a location of the line of cache data and system data from the system input register is placed into the location of the line of cache data after the host data is placed into the addressable memory storage such that the host data is not overwritten. Independent claim 15 is a method claim of similar scope to independent claim 21.

Yet another embodiment of present invention, as set forth by amended independent claim 22, relates to a computer system which includes a host processor, a system memory, a dual port cache memory and a cache controller. The dual port cache memory includes a addressable storage, a host port, a system port, a first and second input registers and first and second output registers. The first input register is coupled between the host port and the addressable storage and is for selectively writing input data to the addressable storage. The first output register is coupled between the addressable storage and the system port and is for selectively furnishing output data to the system port. The input data is provided to the addressable storage from the first input register at the same time that the output data is provided by the first output register to the system port. The second input register is coupled between the addressable storage and the system port and provides second input data to the addressable storage. The second output register is coupled between the addressable storage and the host port and provides second output data from the addressable storage to the host port. The second input data is provided to the addressable storage from the second input register at the same time that the second output data is provided by the second output register to the system port. The cache controller is connected to the dual port cache memory and has a first port connected to the host address bus and a second port connected to the system address bus such that the

cache memory and the cache controller are connected in parallel between the host processor and the system memory. The cache controller provides a first address on the host address bus to the dual port cache memory concurrently with providing a second address on the system address bus; the first address corresponds to a different memory location than the second address.

Regarding independent claim 4, Baldwin does not disclose or suggest a computer system which includes a dual port cache memory coupled between a host processor and a system memory. In fact, as described above, Baldwin does not even describe a cache in the traditional sense of the term. However, even if Baldwin's local memory for his numeric processing subsystem (i.e., "data cache" memory 140) were to be considered a cache, Baldwin does not disclose or suggest a cache memory with dual ports, one connected to a host data bus of the host processor and the other connected to a system data bus of the system memory, all as required by claim 1. For at least this reason, claim 1, and those dependent therefrom, are allowable over Baldwin.

Regarding claim 4 in light of Sachs (which has been made of record, but not relied upon by the Examiner), neither Sachs nor Baldwin, taken alone or in combination, disclose or suggest a computer system including a host processor having a host address bus and a host data bus, a system memory having a system address bus and a system data bus, and a dual port cache memory having registers coupling cache storage locations to a host port and to a system port, wherein a data path between the host data bus and the system data bus is operably decoupled by buffering and selective provision of data to and from the cache storage locations by the registers, so as to allow concurrent transfer of data to and from the dual port cache memory. Buffering and selective provision-related limitations were previously recited in claim 22 and are supported by disclosure which appears, for example, in the abstract. For at least this reason claim 4, and those dependent therefrom, are allowable over Sachs and Baldwin.

Regarding independent claim 21, Baldwin does not disclose or suggest a host input register coupled to addressable memory storage of a dual port cache memory and to

the host data bus for providing data from the host data bus to the addressable memory storage, a system input register coupled to the addressable memory storage and to the system data bus for receiving a line of cache data from the data bus and providing the line of the cache data to the addressable memory storage, and a controller which contains a plurality of addresses corresponding to the cache data for receiving the host address from the host address bus and comparing the host address to the plurality of addresses. Furthermore, Baldwin does not disclose or suggest that when a match results from the comparing, host data from the host input register is placed into the addressable memory storage at a location of the line of cache data and system data from the system input register is placed into the location of the line of cache data after the host data is placed into the addressable memory storage such that the host data is not overwritten, all as required by claim 21. For at least this reason, claim 21, and those dependent therefrom, are allowable over Baldwin. Method claim 15, and those dependent therefrom, are similarly allowable over Baldwin. Claims 21, 15, and those dependent therefrom are similarly allowable over Sachs and Baldwin.

Regarding independent claim 22, the Examiner has rejected the claim in the supplemental Office action (paper 20) without regard to the requirements of 37 C.F.R. 1.106. In particular, the Examiner has rejected claim 22 without identifying disclosure upon which the claim elements allegedly read. In various previous telephonic interviews (two of which were summarized in a paper filed by Applicant May 1, 1996 and a third recorded by the Examiner in paper 19) Applicant respectfully identified the Examiner's prior omission of any consideration of claim 22-32. The supplemental Office action mailed June 18, 1996 includes no substantive consideration and merely adds the claims 22-32 to a list of previously rejected claims, irrespective of any of the specific limitations contained in independent claim 22. Applicant once again respectively requests substantive consideration of claims 22-32. IN THIS REGARD APPLICANT REMAINS ENTITLED TO A NON-FINAL OFFICE ACTION AND TO RECONSIDERATION UNDER 37 C.F.R. 1.112; ANY FINAL REJECTION IN THE NEXT OFFICE ACTION WOULD BE PREMATURE. Regarding allowability of independent claim 22 over

Baldwin, for the reasons described above with reference to claims 1-21, Baldwin does not disclose or suggest a computer system in which a dual port cache memory is coupled between a host processor and a system memory. For at least this reason claim 22, and those dependent therefrom, are allowable over Baldwin.

Additionally, Baldwin does not disclose or suggest a dual port cache memory including a first input register for selectively writing input data to addressable storage and a first output register for selectively furnishing output data to a system port, wherein input data is provided to the addressable storage from the first input register at the same time that output data is provided by the first output register to the system port. Furthermore, Baldwin does not disclose or suggest, the additional features of a cache controller connected to the dual port cache memory for providing a first address on a host address bus concurrently with providing a second address corresponding to a different memory location on a system address bus, a second input register for providing second input data to the addressable storage, and a second output register for providing second output data to a host port, wherein the second input data is provided to the addressable storage from the second input register at the same time that the second output data is provided by the second output register to the system port. For at least each of these reasons, claim 22 is allowable over Baldwin.

Regarding allowability of independent claim 22 over Baldwin and Sachs, neither Baldwin nor Sachs, taken alone or in combination, disclose or suggest a first input register for selectively writing input data to addressable storage and a first output register for selectively furnishing output data to the system port. For at least these reasons, claim 22 and those dependent therefrom are allowable over Baldwin, over Sachs, and over Baldwin and Sachs. Consideration of claims 22-32 is respectfully requested.

Applicant also brings the following commonly-owned U.S. Patent to the Examiner's attention:

(1) U.S. Patent No. 5,488,709 to Chan (inventor of the subject application), issued January 30, 1996 from a continuation-in-part of a common parent application Serial No. 07/546,071.

An Information Disclosure Statement is filed herewith.

CONCLUSION

The claims have been amended to improve clarity, to obtain a more appropriate scope of coverage, and to better distinguish over art made of record but not relied upon by the Examiner. The rejection of claim 21 under 35 U.S.C. § 112 has been addressed through an amendment and the rejections of claims 1-32 under 35 U.S.C. § 103 over Baldwin have been traversed. Claims 4, 15, 21 and 22 have been amended to obtain a more appropriate scope of protection and to better distinguish over art made of record but not relied upon by the Examiner. No new matter has been added.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on October 16, 1996.

10/16/96
Date of Signature

Respectfully submitted,

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(512) 794-3600

EXHIBIT 24

#25/14 PATENT
5-6-97

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Alfred Chan		
Assignee:	MOS Electronics		
Title:	RANDOM ACCESS CACHE MEMORY CONTROLLER AND SYSTEM		
Serial No.:	08/170,642	Filed:	December 20, 1993
Examiner:	Robertson, D.	Group Art Unit:	2318
Atty. Docket No.:	M-1018-3C US		

April 7, 1997

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

This paper is responsive to the Office action mailed January 6, 1997 having a shortened statutory period set to expire April 7, 1997 (April 6, 1997 being a Sunday) and is also responsive to the prior Office action mailed June 18, 1996. Amendments included in the previously filed response were apparently not entered and remarks therein not considered because of a failure to comply with the requirements of 37 C.F.R. 1.121(b). Further to the undersigned's telephonic interview with Examiner Robertson on October 16, 1996, Applicant now resubmits the substance of the prior response with specific parenthetical "amended," "twice amended," and "three times amended" notations. Further examination and reconsideration are respectfully requested in view of the amendments and remarks set forth below.

PROVISIONAL PETITIONS

The Office is provisionally petitioned to extend the shortened statutory period as necessary to avoid abandonment of the Application in relation to the outstanding Office action. If appropriate, a separate Petition for Extension accompanies this Response, this provisional petition being effective in the event that the separate Petition for Extension is defective or missing. The Office is provisionally authorized to charge any amount required to avoid abandonment of the Application in relation to the outstanding Office action to account number 19-2386. A separate Fee Transmittal accompanies this Response, this provisional fee authorization being effective in the event that the separate Fee Transmittal is defective or missing.

AMENDMENTS

In the Claims

Please amend the claims as follows:

4. (three times amended) A computer system comprising:

a host [microprocessor] processor having a host address bus and a host data bus;

a system memory having storage locations addressable by said host processor, a system address bus and a system data bus;

a dual port cache memory having a system port connected to said system data bus [,] and a host port connected to said host data bus, said dual port cache memory comprising [a random access memory] cache storage locations dynamically associable with said storage locations of said system memory and a plurality of registers [connecting] coupling said [random access memory] cache storage locations to said host port and said system port, wherein a data path between said host data bus and said system data bus is operably decoupled by buffering and selective provision of data to and from said [random access memory and] cache storage locations by said

plurality of registers so as to allow concurrent transfer of data to and from said dual port cache memory [cache]; and

a cache controller connected to said dual port cache memory, said cache controller having a first port connected to said host address bus and a second port connected to said system address bus such that said dual port cache memory and said cache controller are connected in parallel between said host [microprocessor] processor and said system memory.

12. (twice amended) The computer system as recited in Claim 1 wherein said cache controller is connected to said dual port cache memory for providing a first address on said host address bus concurrently with providing a second address on said system address bus, said first address corresponding to a different [memory location] one of said storage locations of said system memory than said second address.

13. (amended) The computer system as recited in Claim 1 wherein said host [microprocessor] processor operates at a first frequency, and wherein said system memory operates at a second frequency that is different from said first frequency.

14. (amended) A method for operating a memory cache apparatus, said memory cache apparatus including [a random access memory] addressable storage, a host port, a system port, a host input register connected to said host port, a system input register connected to said system port, and a system output register connected to said system port, said method comprising the steps of:

receiving an address from a host;

comparing said received address to a plurality of addresses corresponding to cache data stored in said [random access memory] addressable storage;

placing a line of said cache data from a location in said [random access memory] addressable storage into said system output register;

placing data from said host into said host input register;

wherein if said received address does not match one of said plurality of [cache addresses] addresses corresponding to said cache data:

placing said host data into said location in said [random access memory] addressable storage from said host input register;

receiving system data corresponding to said received address from said system port into said system input register; and

subsequent to said step of placing said host data into said addressable storage, and without overwriting said host data, placing said system data corresponding to said received address from said system input register into said location in said [random access memory,] addressable storage.

[subsequent to said step of placing said host data into said random access memory, without overwriting said host data.]

12 17. (amended) The method for operating a cache memory apparatus as recited in claim 10 15, wherein data from a plurality of data locations of said [random access memory] addressable storage are placed in said system output register during a single clock cycle.

14 19. (amended) The method for operating a memory cache apparatus as recited in claim 10 15, wherein said step of placing data from said host into said host input register occurs in a first clock cycle, and wherein said step of placing said host data into said location in said [random access memory] addressable storage occurs on a second clock cycle, said second clock cycle immediately following said first clock cycle.

15 21. (twice amended) A computer system comprising:

a host [microprocessor] processor having a host address bus and a host data bus for providing a host address and host data;

a system memory for storing system data, said system memory having a system data bus for providing system data;

a dual port cache memory for storing said host data and system data[;] , said dual port cache memory including:

addressable memory storage;

a host input register [connected to said dual port cache memory and] coupled to said addressable memory storage and to said host data bus for providing data from said host data bus to said [dual port cache memory] addressable memory storage; and

a system input register [connected to said dual port cache memory and] coupled to said addressable memory storage and to said system data bus for receiving a line of said cache data from said data bus and providing said line of cache data to said [dual port cache memory] addressable memory storage; and

a controller connected to said dual port cache memory and said host address bus, said controller containing a plurality of addresses corresponding to said cache data for receiving said host address from said host address bus and comparing said host address to said plurality of addresses[;] , wherein when a match results from said comparing:

host data from said host input register is placed into said [dual port cache memory] addressable memory storage at a location of said line of cache data; and

system data from said system input register is placed into said location of said line of cache data after said host data is placed into said [dual port cache memory] addressable memory storage, wherein said host data is not overwritten.

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22. (amended) A computer system comprising:

a host microprocessor having a host address bus and a host data bus;

a system memory having a system address bus and a system data bus;

a dual port cache memory including:

[a random access memory] addressable storage,
a host port coupled to the host data bus,
a system port coupled to the system data bus,
a first input register for selectively writing input data to said [random access memory] addressable storage, said first input register being coupled between said host port and said [random access memory] addressable storage,
a first output register for selectively furnishing output data to said system port, said first output register being coupled between said [random access memory] addressable storage and said system port, said input data being provided to said [random access memory] addressable storage from said first input register at the same time that said output data is provided by said first output register to said system port,
a second input register for providing second input data to said [random access memory] addressable storage, said second input register being coupled between said [random access memory] addressable storage and said system port, and
a second output register coupled between said [random access memory] addressable storage and said host port for providing second output data from said [random access memory] addressable storage to said host port, said second input data being provided to said [random access memory] addressable storage from said second input register at the same time that said second output data is provided by said second output register to said system port; and
a cache controller connected to said dual port cache memory, said cache controller having a first port connected to said host address bus and a second port connected to said system address bus such that said cache memory and

said cache controller are connected in parallel between said host [microprocessor] processor and said system memory,

said cache controller being connected to said dual port cache memory for providing a first address on said host address bus concurrently with providing a second address on said system address bus, said first address corresponding to a different memory location than said second address.

REMARKS

Claim 21 was rejected under 35 U.S.C. § 112, second paragraph. The Examiner stated that "'said data bus' lacks proper antecedent basis." Claim 21 has been amended to provide proper antecedent basis. Further consideration is requested.

The Examiner rejected claims 4, 15, 21, 22, and those dependent therefrom (i.e., 4-11 and 15-32) under 35 U.S.C. § 103 as being unpatentable over United States Patent No. 5,329,630 to Baldwin. This rejection is traversed. Applicant respectfully suggests that the prior Examiner's interpretation of Baldwin is not in accordance with the disclosure thereof. However, claims 4, 15, and 21 have been amended to obtain a more appropriate scope of coverage and to better distinguish over art made of record but not relied upon by the Examiner (e.g., Sachs et al.). Claims 5, 11, 17, 19, and 22 have been amended to obtain a more appropriate scope of coverage.

Regarding the art relied upon by the Examiner, Baldwin discloses a double buffering system wherein a dual port memory is partitioned in software so that the top half of the memory is allocated to one processor and the bottom half to the other. The double buffering is implemented by switching the allocation under control of the two processors. *See* Baldwin, Abstract. Baldwin's data cache memory 140 is a cache in name only. In reality, data cache memory 140 is merely a small, wide, fast memory for use in a numeric processing subsystem of a larger computer system. *See* Baldwin, Col. 9, lines 14-37. Data cache memory 140 does not function as a cache providing a processor with high speed access to frequently used memory locations while accesses to uncached

locations are serviced by a lower speed memory device. Instead, data cache memory 140 is loaded with data in response to commands from a host processor external to the numeric processing subsystem. *See* Baldwin, Col. 106, line 6 - Col. 107, line 66. Both the host processor and system memory reside on a VME-bus (*see* Baldwin, Figs. 34-37, and 41) which couples to the numeric processing subsystem of Fig. 1 via host (or VME) external interface controller 160 (*see* Baldwin, Col. 10, lines 16-30).

Several points are made clear by Baldwin's discussion of his physical memory model in the context of a host processor command to the numeric processing subsystem to multiply two arrays and store the results in a third array, wherein all three arrays reside in VME memory space. First, data cache memory 140 is not a cache in the traditional sense of the term. Second, the "processors" to which data cache is coupled are themselves tightly coupled in their respective numeric, control, and data transfer functions, interrupting each other to gain access to resources including data cache 140. Third, both the host processor and the system memory are external to the numeric processing subsystem, i.e., reside on a VME bus across external (VME) interface 160 from the numeric processing subsystem and "data cache" memory 140. *See* Baldwin, Col. 106, line 6 - Col. 107, line 66. In short, data cache memory 140 can not be said to be a cache in the traditional sense, floating point processor is not a host processor initiating loads and stores to addresses in an address space greater than that represented in "data cache" memory 140, and neither a host processor nor system memory resides on the numeric processor side (i.e., "data cache" side) of the an external VME interface.

United States Patent No. 5,091,846 to Sachs, et al. has been made of record but not relied upon by the Examiner. Applicant wishes the Examiner to consider Sachs et al. in light of the following. Sachs et al. disclose a cache memory management unit which includes a cache memory subsystem 220 which is coupled to a cache bus via cache output register 230 and cache input register 240 and is coupled to a system bus via system bus input register 260 and system bus output register 250. The cache output register is directly coupled via a data out line to the memory subsystem. The cache input register, system bus

input register and system bus output register are coupled to the memory subsystem via a data bus 241.

In contrast with both of the above-described references, an embodiment of the present invention, as set forth by amended independent claim 4, relates to a computer system which includes a host processor, a system memory, a dual port cache memory, and a cache controller. The host processor has a host address bus and a host data bus. The system memory has storage locations addressable by the host processor and has a system address bus and a system data bus. The dual port cache memory includes cache storage locations dynamically associable with the storage locations of the system memory, a host port, a system port, and a plurality of registers coupling the cache storage locations to the host port and the system port. The system port is connected to the system data bus and the host port is connected to the host data bus. A data path between the host data bus and the system data bus is operably decoupled by buffering and selective provision of data to and from the cache storage locations by the registers, allowing concurrent transfer of data to and from the dual port cache memory.

Another embodiment of present invention, as set forth by amended independent claim 21, is of similar scope to independent claim 4 but specifies a host input register coupled to the addressable memory storage of the dual port cache memory and to the host data bus for providing data from the host data bus to the addressable memory storage; a system input register coupled to the addressable memory storage and to the system data bus for receiving a line of cache data from the data bus and providing the line of the cache data to the addressable memory storage, and a controller which contains a plurality of addresses corresponding to the cache data for receiving the host address from the host address bus and comparing the host address to the plurality of addresses. When a match results from the comparing, host data from the host input register is placed into the addressable memory storage at a location of the line of cache data and system data from the system input register is placed into the location of the line of cache data after the host data is placed into the addressable memory storage such that the host data is not

overwritten. Independent claim 15 is a method claim of similar scope to independent claim 21.

Yet another embodiment of present invention, as set forth by amended independent claim 22, relates to a computer system which includes a host processor, a system memory, a dual port cache memory and a cache controller. The dual port cache memory includes a addressable storage, a host port, a system port, a first and second input registers and first and second output registers. The first input register is coupled between the host port and the addressable storage and is for selectively writing input data to the addressable storage. The first output register is coupled between the addressable storage and the system port and is for selectively furnishing output data to the system port. The input data is provided to the addressable storage from the first input register at the same time that the output data is provided by the first output register to the system port. The second input register is coupled between the addressable storage and the system port and provides second input data to the addressable storage. The second output register is coupled between the addressable storage and the host port and provides second output data from the addressable storage to the host port. The second input data is provided to the addressable storage from the second input register at the same time that the second output data is provided by the second output register to the system port. The cache controller is connected to the dual port cache memory and has a first port connected to the host address bus and a second port connected to the system address bus such that the cache memory and the cache controller are connected in parallel between the host processor and the system memory. The cache controller provides a first address on the host address bus to the dual port cache memory concurrently with providing a second address on the system address bus; the first address corresponds to a different memory location than the second address.

Regarding independent claim 4, Baldwin does not disclose or suggest a computer system which includes a dual port cache memory coupled between a host processor and a system memory. In fact, as described above, Baldwin does not even describe a cache in

the traditional sense of the term. However, even if Baldwin's local memory for his numeric processing subsystem (i.e., "data cache" memory 140) were to be considered a cache, Baldwin does not disclose or suggest a cache memory with dual ports, one connected to a host data bus of the host processor and the other connected to a system data bus of the system memory, all as required by claim 1. For at least this reason, claim 1, and those dependent therefrom, are allowable over Baldwin.

Regarding claim 4 in light of Sachs (which has been made of record, but not relied upon by the Examiner), neither Sachs nor Baldwin, taken alone or in combination, disclose or suggest a computer system including a host processor having a host address bus and a host data bus, a system memory having a system address bus and a system data bus, and a dual port cache memory having registers coupling cache storage locations to a host port and to a system port, wherein a data path between the host data bus and the system data bus is operably decoupled by buffering and selective provision of data to and from the cache storage locations by the registers, so as to allow concurrent transfer of data to and from the dual port cache memory. Buffering and selective provision-related limitations were previously recited in claim 22 and are supported by disclosure which appears, for example, in the abstract. For at least this reason claim 4, and those dependent therefrom, are allowable over Sachs and Baldwin.

Regarding independent claim 21, Baldwin does not disclose or suggest a host input register coupled to addressable memory storage of a dual port cache memory and to the host data bus for providing data from the host data bus to the addressable memory storage, a system input register coupled to the addressable memory storage and to the system data bus for receiving a line of cache data from the data bus and providing the line of the cache data to the addressable memory storage, and a controller which contains a plurality of addresses corresponding to the cache data for receiving the host address from the host address bus and comparing the host address to the plurality of addresses. Furthermore, Baldwin does not disclose or suggest that when a match results from the comparing, host data from the host input register is placed into the addressable memory

storage at a location of the line of cache data and system data from the system input register is placed into the location of the line of cache data after the host data is placed into the addressable memory storage such that the host data is not overwritten, all as required by claim 21. For at least this reason, claim 21, and those dependent therefrom, are allowable over Baldwin. Method claim 15, and those dependent therefrom, are similarly allowable over Baldwin. Claims 21, 15, and those dependent therefrom are similarly allowable over Sachs and Baldwin.

Regarding independent claim 22, the prior Examiner (Elmore) rejected the claim in the supplemental Office action (paper 20) without regard to the requirements of 37 C.F.R. 1.106. In particular, and as highlighted in the prior response, the prior Examiner rejected claim 22 without identifying disclosure upon which the claim elements allegedly read. In various previous telephonic interviews (two of which were summarized in a paper filed by Applicant May 1, 1996 and a third recorded by the prior Examiner in paper 19), Applicant respectfully identified the prior Examiner's prior omission of any consideration of claims 22-32. The supplemental Office action mailed June 18, 1996 included no substantive consideration and merely added the claims 22-32 to a list of previously rejected claims, irrespective of any of the specific limitations contained in independent claim 22. The Office Action mailed January 6, 1997 does not alter this status. Applicant appreciates the opportunity to conform the previously submitted response to the requirements of 37 C.F.R. 1.121 and once again respectively requests substantive consideration of claims 22-32.

BECAUSE APPLICANT HAS NOT YET BEEN AFFORDED SUBSTANTIVE CONSIDERATION OF CLAIMS 22-32, APPLICANT REMAINS ENTITLED TO A NON-FINAL OFFICE ACTION AND TO RECONSIDERATION UNDER 37 C.F.R. 1.112; ANY FINAL REJECTION IN THE NEXT OFFICE ACTION WOULD BE PREMATURE. Regarding allowability of independent claim 22 over Baldwin, for the reasons described above with reference to claims 1-21, Baldwin does not disclose or suggest a computer system in which a dual port cache memory is coupled between a host

processor and a system memory. For at least this reason claim 22, and those dependent therefrom, are allowable over Baldwin.

Additionally, Baldwin does not disclose or suggest a dual port cache memory including a first input register for selectively writing input data to addressable storage and a first output register for selectively furnishing output data to a system port, wherein input data is provided to the addressable storage from the first input register at the same time that output data is provided by the first output register to the system port. Furthermore, Baldwin does not disclose or suggest, the additional features of a cache controller connected to the dual port cache memory for providing a first address on a host address bus concurrently with providing a second address corresponding to a different memory location on a system address bus, a second input register for providing second input data to the addressable storage, and a second output register for providing second output data to a host port, wherein the second input data is provided to the addressable storage from the second input register at the same time that the second output data is provided by the second output register to the system port. For at least each of these reasons, claim 22 is allowable over Baldwin.

Regarding allowability of independent claim 22 over Baldwin and Sachs, neither Baldwin nor Sachs, taken alone or in combination, disclose or suggest a first input register for selectively writing input data to addressable storage and a first output register for selectively furnishing output data to the system port. For at least these reasons, claim 22 and those dependent therefrom are allowable over Baldwin, over Sachs, and over Baldwin and Sachs. Consideration of claims 22-32 is respectfully requested.

Applicant also brings the following commonly-owned U.S. Patent to the Examiner's attention:

(1) U.S. Patent No. 5,488,709 to Chan (inventor of the subject application), issued January 30, 1996 from a continuation-in-part of a common parent application Serial No. 07/546,071.

An Information Disclosure Statement accompanied the prior filed response.

CONCLUSION

The claims have been amended to improve clarity, to obtain a more appropriate scope of coverage, and to better distinguish over art made of record but not relied upon by the Examiner. The rejection of claim 21 under 35 U.S.C. § 112 has been addressed through an amendment and the rejections of claims 1-32 under 35 U.S.C. § 103 over Baldwin have been traversed. Claims 4, 15, and 21 have been amended to obtain a more appropriate scope of protection and to better distinguish over art made of record but not relied upon by the Examiner. Claims 5, 11, 17, 19, and 22 have been amended to obtain a more appropriate scope of coverage. No new matter has been added.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on April 7, 1997.

4,7,97
Date of Signature

Respectfully submitted,

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EXHIBIT 25

08/170642

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/170,642	12/20/93	CHAN	A M10183C

EXAMINER	
ELMORE, R	
ART UNIT	**PAPER NUMBER**
2318	20

B3M1/0618

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DATE MAILED: 06/18/96

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to telephone communication ~~filed on~~ 6-10-96 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 4-11 & 15-32 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☒ Claims 1-3 & 12-14 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 4-11 & 15-32 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

1. This office action replaces the office action, paper #17. As detailed in the interview summary, paper # 19, claims 22-32, presented in the preliminary amendment filed 12-20-93, were not included in the previous rejection. This office action includes all claims currently presented for examination.

2. Claims 4-11 and 15-32 are presented for examination.

3. The changes to Figures 8B and 8C are approved by the examiner, however, applicant is reminded of the provisions of MPEP 608.02(q) and 608.02(r) regarding a separate draftsman's letter.

4. Claim 21 is rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim is indefinite because:

(a) "said data bus" lacks proper antecedent basis, a host data bus and a system data bus have been previously claimed, it is not clear which data bus 'said data bus' is referencing -- claim 21, lines 13-14.

5. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

> Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

6. Claims 4-11 and 15-32 are rejected under 35 USC § 103 as being unpatentable over Baldwin et al.

Baldwin teaches the invention (claims 4, 15, 21 and 22) substantially as claimed, including a computer system and method for operation a memory cache apparatus, the system and method comprising:

(a) a host microprocessor having a host address bus and a host data bus (e.g., see col. 9, lines 39-52 and Figure 1);

(b) an input register connected to the cache memory and the host data bus (e.g., see col. 50, lines 33-42);

(c) a system memory having a system address bus and a system data bus (e.g., see Figures 34-37, 41);

(d) a tri-port cache memory which essentially functions as a dual port cache memory and connects to a system bus and a host bus (e.g., see col. 15, lines 45-62); and,

(e) an input register connected to the dual port cache memory and the system data bus (e.g., see col. 67, line 47 to col. 70, line 30).

Baldwin does not specifically teach a cache controller connected to the dual port cache memory, however, functions

performed by a cache controller are performed by the three processors connected to the data cache memory (e.g., see col. 15, line 17 to col. 16, line 11). It would have been obvious to one of ordinary skill in the art of memory storage at the time the invention was made to equate the functions of the processor modules to the functions of a cache controller because the processor modules perform the data control and transfer tasks typically performed by a cache controller.

As to claims 5 and 16-17, Baldwin teaches the host processor concurrently processing tasks with access the cache memory with the other processors of the system (e.g., see col. 1, lines 29-52).

As to claims 6 and 23, Baldwin teaches the host data bus is asynchronous to the system data bus (e.g., see col. 1, lines 38-41).

As to claims 7 and 24, Baldwin teaches control sequencing of addresses and data signals (e.g., see col. 20, line 63 to col. 21, line 51).

As to claims 8 and 25, Baldwin teaches local bus cycles (e.g., see col. 15, lines 45-62).

As to claims 9-10 and 26-27, Baldwin teaches a peripheral device coupled to the system which provides data to the cache (e.g., see col. 16, lines 25-62).

As to claims 11 and 28, Baldwin teaches sub-systems operating using different parameters (e.g., see col. 3, line 27 to col. 6,line 15).

As to claims 18-20, Baldwin teaches data is moved to/from the cache by the processors during clock cycles (e.g., see col. 15, line 15 to col. 16, line 24).

As to claim 29, Baldwin teaches data transfer between a dual port memory and the processor to the extent claimed (e.g., see col. 2, lines 19-46 and Figures 18 and 19).

As to claims 30-31, Baldwin teaches logic for using registers for read holding, write holding or write through. The registers can also be used to hold update data (e.g., see col. 39, lines 25-35 and col. 46, line 1 to col. 47, line 48).

As to claim 32, Baldwin teaches write masking to the extent claimed (e.g., see col. 66, line 58 to col. 67, line 17).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba. I. Elmore whose telephone number is (703) 305-3819.

The examiner can normally be reached on Monday-Thursday from 6:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tod R. Swann, can be reached on (703) 308-7791. The fax phone number for this Group is (703) 305-9565.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Reba I. Elmore
Primary Examiner
June 15, 1996

EXHIBIT 26

IBM DICTIONARY OF COMPUTING

Compiled and edited by

GEORGE McDANIEL

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2 3 4 5 6 7 8 9 0 DOC/DOC 9 9 8 7 6 5 4

ISBN 0-07-031488-8 (HC)
ISBN 0-07-031489-6 (PBK)

The sponsoring editor for this book was Daniel A. Gonneau and the production supervisor was Thomas G. Kowalczyk.

Printed and bound by R. R. Donnelley & Sons Company.

Tenth Edition (August 1993)

This is a major revision of the *IBM Dictionary of Computing*, SC20-1699-8, which is made obsolete by this edition. Changes are made periodically to the information provided herein.

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information in the form of messages to the user from client applications that are currently running.

bumping up In video applications, the process of transferring recorded video to a higher-quality tape format, such as from a half-inch tape to three-quarter-inch tape.

burned-in address See hard address.

burn in A process of increasing the reliability performance of hardware employing functional operation of every functional unit in a prescribed environment with successive corrective maintenance at every failure during the early failure period. (T)

burnt-in time code In videotaping, the time of day as displayed in a window on a videotape.

burst (1) In data communication, a sequence of signals counted as one unit in accordance with some specific criterion or measure. (A) (2) To separate continuous-form paper into discrete sheets. (A) (3) See error burst.

burster A device to detach from one another previously-perforated forms or formsets of continuous stationery. (T)

burster-trimmer-stacker (BTS) A printer feature that bursts continuous forms into separate sheets, trims the carrier strip from both edges of the forms, and stacks single sheets. See also job offset.

burst isochronous transmission Synonym for burst transmission.

burst mode A mode in which data is transmitted by means of burst transmission.

burst noise In acoustics, noise characterized by acoustic impulses that significantly exceed the level of ambient noise.

burst pages On continuous-form paper, pages of output that can be separated at the perforations.

burst transmission (1) Data transmission at a specific data signalling rate during controlled intermittent intervals. (I) (A) (2) Synonymous with burst isochronous transmission, interrupted isochronous transmission.

bus (1) A facility for transferring data between several devices located between two end points, only one device being able to transmit at a given moment. (T) (2) A computer configuration in which processors are interconnected in series. See also hypercube. (3) One or more conductors used for transmitting signals or power. (A) (4) See bidirectional bus, control bus, data bus. See also bus network.

bus extension card (BEC) In the AS/400 system, the bus extension driver card or the bus extension receiver card.

bus extension driver (BED) card In the AS/400 system, the card, connected by a cable to a bus extension receiver (BER) card, that is used to route data from one card enclosure to another card enclosure. The direction of data can be from the processing unit to an input/output processor in one of the card enclosures, or from an input/output processor in one of the card enclosures to the processing unit. See also bus extension receiver (BER) card.

bus extension receiver (BER) card In the AS/400 system, the card, connected by a cable to a bus extension driver (BED) card, that is used to route data from one card enclosure to another card enclosure. The direction of data can be from the processing unit to an input/output processor in one of the card enclosures, or from an input/output processor in one of the card enclosures to the processing unit. See also bus extension driver (BED) card.

business area A product area where business is performed.

business graphics See graphics.

business graphics utility (BGU) An IBM-supplied OFFICE/38 utility that provides a menu-driven means of using the System/38 chart functions without knowledge of programming.

business machine (1) A machine designed to facilitate clerical operations in commercial or scientific activities. (2) Customer-provided data terminal equipment (DTE) that connects to telecommunication equipment of a communication common carrier, a Recognized Private Operating Agency, or a telecommunication Administration, for the purpose of data transfer. See also COAM equipment.

business machine clocking A time base oscillator supplied by the business machine for regulating the bit rate of transmission. Synonymous with non-data-set clocking. Contrast with data set clocking.

business partner Any non-IBM organization, with whom IBM has a written contract defining a complementary marketing relationship, that provides end users with information-handling solutions that use or rely upon an IBM offering.

bus master A device or subsystem that controls data transfers between itself and a slave.

clicking a mouse button, and then disappears when the action is completed.

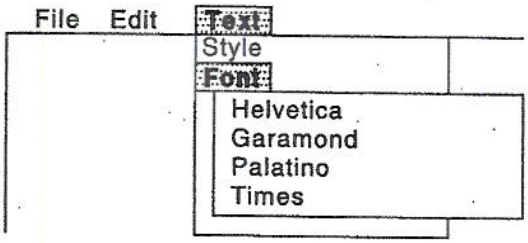

Figure 115. Pop-up Menu

pop-up widget In AIX Enhanced X-Windows, a window child of the root that is attached to its widget parent differently than the normal widget; a pop-up widget is not geometrically constrained by its parent widget.

pop-up window In SAA Advanced Common User Access architecture, a movable window, fixed in size, in which a user provides information required by an application so that it can continue to process a user request.

port (1) An access point for data entry or exit. (2) A connector on a device to which cables for other devices such as display stations and printers are attached. Synonymous with socket. See communication port, game port, I/O port, parallel port, serial port, terminal port. (3) A specific communications end point within a host. A port is identified by a port number. (4) The representation of a physical connection to the link hardware. A port is sometimes referred to as an adapter; however, there can be more than one port on an adapter. There may be one or more ports controlled by a single DLC process. (5) To make the programming changes necessary to allow a program that runs on one type of computer to run on another type of computer. (6) Deprecated term for adapter. (7) See delayed port, disabled port, protocol port, serial port, shared port, textport. (8) See also viewport.

portability (1) The capability of a program to be executed on various types of data processing systems without converting it to a different language and with little or no modification. (T) (2) The ability to transport equipment manually. (3) The ability to run a program on more than one computer without modifying it. (4) Synonymous with transportability. See data portability.

portable computer A microcomputer that can be hand carried for use in more than one location. (T)

portable dictation machine A dictation machine having a self-contained power supply and designed primarily for easy movement from one place to another. (I)

portable typewriter A typewriter designed primarily for easy movement from one place to another. It is usually supplied with a carrying case that also serves to protect the machine while it is being moved. (T)

port address In an ESCON Director, an address used to specify port connectivity parameters and to assign link addresses for attached channels and control units. See also link address.

port address name In an ESCON Director, a user-defined symbolic name of 24 characters or less that identifies a particular port.

Port-A-Punch equipment Portable punching equipment manufactured by IBM.

port card In an ESCON environment, a field-replaceable hardware component that provides the opto-mechanical attachment method for jumper cables and performs specific device-dependent logic functions.

port designation A 4-character identifier (such as LPT1 or COM1) assigned to a printer, plotter, or communications device so that the system has a unique way to refer to the resource.

portfolio In multimedia, a series of timed video stills, producing a "slide show" effect.

port group A group of ports identified by the common carrier with a single data terminal equipment (DTE) address. The network directs incoming calls to the first available port, using a sequential search technique.

port information block (PIB) In an ESCON Director, a data area that contains information relating to the connectivity of each available port.

port number (1) In an ESCON Director, a hexadecimal number that identifies a physical link connection point. This number is identical to its port address unless the service representative has reassigned the port associated with that address. (2) In TCP/IP, a 16-bit number used to communicate between TCP and a higher-level protocol or application. Some protocols, such as the File Transfer Protocol (FTP) and the Simple Mail Transfer Protocol (SMTP), use the same port number in all TCP/IP implementations. See well-known port.

portrait (1) The arrangement of text on a page so that it is oriented for normal reading when its length is

repeatedly producing a display image on a display surface so that the image remains visible. (I) (A) (3) To recharge a memory location in volatile memory with an electric current so that it retains a state or binary value. (4) See system refresh.

Refresh In SAA Basic Common User Access architecture, an action that updates the information that a user is currently looking at.

refreshable The attribute of a load module that prevents it from being modified by itself or by any other module during execution. A refreshable load module can be replaced by a new copy during execution by a recovery management routine without changing either the sequence or results of processing.

refreshable program A program that can be replaced at any time with a new copy without changing either the sequence or results of processing.

refresh rate (1) The number of times per second that a display image is produced for refresh. (I) (A) (2) In word processing, the rate at which a displayed image is renewed in order to appear stable. (T)

regenerate (1) To restore information to its original state. (2) To recharge a dissipating storage device to its fully charged state.

regeneration (1) In computer graphics, the sequence of events needed to generate a display image from its representation in storage. (I) (A) (2) The restoration of stored information. (3) See signal regeneration.

regenerative track Part of a track on a magnetic drum or magnetic disk used in conjunction with a read head and a write head that are connected to function as a circulating storage. (A) Synonymous with revolver track.

region A variable-size subdivision of a dynamic area that is allocated to a job step or a system task.

regional center A control center (class 1 office) connecting sectional centers of the telephone system together. Every pair of regional centers in the United States has a direct circuit group running from one center to the other.

region class In IMS/VS, the class assigned to a message region to indicate the message classes that can be processed within the region. See also message class.

region control task (RCT) In TSO, the control program routine that handles quiesce/restore and LOGON/LOGOFF.

region job pack area (JPA) In OS/VS2, an area in a virtual region that contains modules that are not in the link pack area but are needed for the execution of jobs.

region size The amount of main storage available for a program to run. See also job region, step region.

register (1) A part of internal storage having a specified storage capacity and usually intended for a specific purpose. (T) (2) In DPCX, a field capable of containing 10 digits, a sign, and a decimal point, that can be used by a program for arithmetic calculations and for program control. (3) On a document copying machine, to accurately position the image of the original on the copy material. (T)

registered network ID An 8-byte name included in an IBM-maintained worldwide registry that has a structured format and is assigned to a particular IBM customer to uniquely identify a specific network.

register guides In a document copying machine, indicators on or near the platen that help position the original correctly. (T)

register insertion In a ring network configuration, a ring control scheme in which each station loads the frame it is transmitting into a shift register and, when the ring is idle, inserts the entire contents of the register into the ring. The sending station removes the register contents from the ring when it is returned by the receiving station. See also master node control, slotted-ring control, token-access control.

register length The storage capacity of a register. (I) (A)

registrable resource A logical unit that can be registered with a network node server, a central directory server, or both.

registration (1) The accurate positioning of an entity relative to a reference. (A) (2) On a document copying machine, the consistency of register on successive copies. (T) (3) In a duplicator, the consistency of the relative position of images printed on paper. (T) (4) In X.25, the process used between a data terminal equipment (DTE) and a data circuit-terminating equipment (DCE) to establish an agreement on which optional user facilities will be in effect; for example, the DTE can request that the DCE agree to or stop a previous agreement for an optional user facility. Also, a DCE can indicate the optional user facilities that are available or the optional user facilities that are currently in effect. The negotiation is accomplished through the exchange of registration packets. (5) In the ImagePlus system, the final step in the process of storing an object. Registration represents a positive identification of the object based on the

EXHIBIT 27

Microsoft Press

Computer Dictionary

Third Edition

Microsoft® Press

PUBLISHED BY
Microsoft Press
A Division of Microsoft Corporation
One Microsoft Way
Redmond, Washington 98052-6399

Library of Congress Cataloging-in-Publication Data
Microsoft Press Computer Dictionary. -- 3rd ed.
p. cm.
ISBN 1-57231-446-X
1. Computers--Dictionaries. 2. Microcomputers--Dictionaries.
I. Microsoft Press.
QA76.15.M54 1997
004'.03--dc21 97-15489
CIP

Printed and bound in the United States of America.

1 2 3 4 5 6 7 8 9 QMQM 2 1 0 9 8 7

Distributed to the book trade in Canada by Macmillan of Canada, a division of Canada Publishing Corporation.

A CIP catalogue record for this book is available from the British Library.

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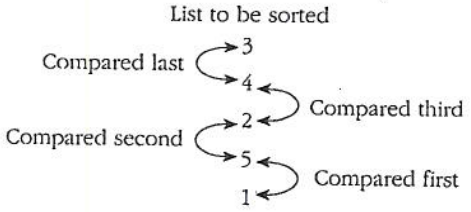
bubble memory \bub´l mem`ər-ē\ *n.* Memory formed by a series of persistent magnetic "bubbles" in a thin film substrate. In contrast to ROM, information can be written to bubble memory. In contrast to RAM, data written to bubble memory remains there until it is changed, even when the computer is turned off. For this reason, bubble memory has had some application in environments in which a computer system must be able to recover with minimal data loss in the event of a power failure. The use of and demand for bubble memory has all but disappeared because of the introduction of flash memory, which is less expensive and easier to produce. *See also* flash memory, nonvolatile memory.

bubble sort \bub´l sōrt`\ *n.* A sorting algorithm that starts at the end of a list with *n* elements and moves all the way through, testing the value of each adjacent pair of items and swapping them if they aren't in the right order. The entire process is then repeated for the remaining $n - 1$ items in the list, and so on, until the list is completely sorted, with the largest value at the end of the list. A bubble sort is so named because the "lightest" item in a list (the smallest) will figuratively "bubble up" to the top of the list first; then the next-lightest item bubbles up to its position, and so on. See the illustration. *Also called* exchange sort. *See also* algorithm, sort. *Compare* insertion sort, merge sort, quicksort.



List after first pass	List after second pass
1	1
3	2
4	3
2	4
5	5

Bubble sort.

bubble storage \bub´l stōr`əj\ *n.* *See* bubble memory.

bucket \buk´ət\ *n.* A region of memory that is addressable as an entity and can be used as a receptacle to hold data. *See also* bit bucket.

buffer[1] \buf´ər\ *n.* A region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations, as between an application's data area and an input/output device. A device or its adapter may in turn use a buffer to store data awaiting transfer to the computer or processing by the device.

buffer[2] \buf´ər\ *vb.* To use a region of memory to hold data that is waiting to be transferred, especially to or from input/output (I/O) devices such as disk drives and serial ports.

buffer pool \buf´ər pōōl`\ *n.* A group of memory or storage-device locations that are allocated for temporary storage, especially during transfer operations.

buffer storage \buf´ər stōr`əj\ *n.* **1.** The use of a special area in memory to hold data temporarily for processing until a program or operating system is ready to deal with it. **2.** An area of storage that is used to hold data to be passed between devices that are not synchronized or have different bit transfer rates.

bug \bug\ *n.* **1.** An error in coding or logic that causes a program to malfunction or to produce incorrect results. Minor bugs, such as a cursor that does not behave as expected, can be inconvenient or frustrating, but do not damage information. More severe bugs can require the user to restart the program or the computer, losing whatever previous work had not been saved. Worse yet are bugs that damage saved data without alerting the user. All such errors must be found and corrected by the process known as *debugging.* Because of the potential risk to important data, commercial application programs are tested and debugged as completely as possible before release. After the program becomes available, further minor bugs are corrected in the next update. A more severe bug can sometimes be fixed with a piece of software called a *patch,* which circumvents the problem or in some other way alleviates its effects. *See also* beta test,

high-speed data stream, becomes a channel dedicated to the needs of one device until the entire transmission has been sent. Burst mode is used both in communications and between devices in a computer system. *See also* burst[1].

burst rate \burst´ rāt\ *n.* *See* burst speed (definition 1).

burst speed \burst´ spēd\ *n.* **1.** The fastest speed at which a device can operate without interruption. For example, various communications devices (as on networks) can send data in bursts, and the speed of such equipment is sometimes measured as the burst speed (the speed of data transfer while the burst is being executed). *Also called* burst rate. **2.** The number of characters per second that a printer can print on one line without a carriage return or linefeed. Burst speed measures the actual speed of printing, without consideration of the time taken to advance paper or to move the print head back to the left margin. Almost always, the speed claimed by the manufacturer is the burst speed. By contrast, *throughput* is the number of characters per second when one or more entire pages of text are being printed and is a more practical measurement of printer speed in real-life situations.

bursty \bur´stē\ *adj.* Transmitting data in spurts, or bursts, rather than in a continuous stream.

bus \bus\ *n.* A set of hardware lines (conductors) used for data transfer among the components of a computer system. A bus is essentially a shared highway that connects different parts of the system—including the microprocessor, disk-drive controller, memory, and input/output ports—and enables them to transfer information. The bus consists of specialized groups of lines that carry different types of information. One group of lines carries data; another carries memory addresses (locations) where data items are to be found; yet another carries control signals. Buses are characterized by the number of bits they can transfer at a single time, equivalent to the number of wires within the bus. A computer with a 32-bit address bus and a 16-bit data bus, for example, can transfer 16 bits of data at a time from any of 2^{32} memory locations. Most microcomputers contain one or more expansion slots into which additional boards can be plugged to connect them to the bus.

bus enumerator \bus´ ə-nōō`mər-ā-tər\ *n.* A device driver that identifies devices located on a specific bus and assigns a unique identification code to each device. The bus enumerator is responsible for loading information about the devices onto the hardware tree. *See also* bus, device driver, hardware tree.

bus extender \bus´ eks-ten`dər\ *n.* **1.** A device that expands the capacity of a bus. For example, IBM PC/AT computers used a bus extender to add onto the earlier PC bus and allow the use of 16-bit expansion boards in addition to 8-bit boards. *See also* bus. **2.** A special board used by engineers to raise an add-on board above the computer's cabinet, making it easier to work on the circuit board.

business graphics \biz´nəs graf`iks\ *n.* *See* presentation graphics.

business information system \biz`nəs in-fər-mā´shən si`stəm\ *n.* A combination of computers, printers, communications equipment, and other devices designed to handle data. A completely automated business information system receives, processes, and stores data; transfers information as needed; and produces reports or printouts on demand. *Acronym:* BIS (B`I-S´). *See also* management information system.

business software \biz´nəs soft`wâr\ *n.* Any computer application designed primarily for use in business, as opposed to scientific use or entertainment. In addition to the well-known areas of word processing, spreadsheets, databases, and communications, business software for microcomputers also encompasses such applications as accounting, payroll, financial planning, project management, decision and support systems, personnel record maintenance, and office management.

bus mouse \bus´ mous\ *n.* A mouse that attaches to the computer's bus through a special card or port rather than through a serial port. *See also* mouse. *Compare* serial mouse.

bus network \bus´ net`wərk\ *n.* A topology (configuration) for a local area network in which all nodes are connected to a main communications line (bus). On a bus network, each node monitors activity on the line. Messages are detected by all nodes but are accepted only by the node(s) to which they are addressed. A malfunctioning node ceases to communicate but does not disrupt oper-

smaller than a postage stamp and require only a few milliwatts of power. *See also* integrated circuit.

microfiche \mī´krō-fēsh`\ *n.* A small sheet of film, about 4 by 6 inches, used for recording photographically reduced images, such as document pages, in rows and columns forming a grid pattern. The resulting images are too small to read with the naked eye, and a microfiche reader is required to view the documents. *Compare* microfilm.

microfilm \mī´krō-film`\ *n.* A thin strip of film stored on a roll and used to record sequential data images. As with microfiche, a special device magnifies the images so that they can be read. *See also* CIM (definition 2), COM (definition 4). *Compare* microfiche.

microfloppy disk \mī`krō-flop´ē disk\ *n.* A 3.5-inch floppy disk of the type used with the Apple Macintosh and with IBM and compatible microcomputers. A microfloppy disk is a round piece of polyester film coated with ferric oxide and encased in a rigid plastic shell equipped with a sliding metal cover. On the Macintosh, a single-sided microfloppy disk can hold 400 kilobytes (KB); a double-sided (standard) disk can hold 800 KB; and a double-sided high-density disk can hold 1.44 megabytes (MB). On IBM and compatible machines, a microfloppy can hold either 720 KB or 1.44 MB of information. *See also* floppy disk.

microform \mī´krō-fōrm`\ *n.* The medium, such as microfilm or microfiche, on which a photographically reduced image, called a *microimage*, is stored. A microimage usually represents text, such as archived documents. *See also* microfiche, microfilm.

micrographics \mī`krō-graf´iks\ *n.* The techniques and methods for recording data on microfilm. *See also* microform.

microimage \mī´krō-im`əj\ *n.* A photographically reduced image, usually stored on microfilm or microfiche, that is too small to be read without magnification. *See also* microform, micrographics.

microinstruction \mī´krō-in-struk`shən\ *n.* An instruction that is part of the microcode. *See also* microcode.

microjustification \mī`krō-ju-stə-fə-kā´shən\ *n.* *See* microspace justification.

microkernel \mī´krō-kər`nəl\ *n.* **1.** In programming, the strictly hardware-dependent part of an operating system that is intended to be portable from one type of computer to another. The microkernel provides a hardware-independent interface to the rest of the operating system, so only the microkernel needs to be rewritten to port the operating system to a different platform. *See also* kernel, operating system. **2.** A kernel that has been designed with only the basic features and typically in a modular fashion.

micrologic \mī´krō-loj`ik\ *n.* A set of instructions, stored in binary form, or a set of electronic logic circuits that defines and governs the operation within a microprocessor.

microminiature \mī`krō-min´ə-chur\ *n.* An extremely small circuit or other electronic component, especially one that is a refinement of an already miniaturized element.

microphone \mī´krə-fōn`\ *n.* **1.** A device that converts sound waves into analog electrical signals. Additional hardware can convert the microphone's output into digital data that a computer can process; for example, to record multimedia documents or analyze the sound signal. **2.** A communications program that runs on the Apple Macintosh computer.

microprocessor \mī`krō-pros´es-ər\ *n.* A central processing unit (CPU) on a single chip. A modern microprocessor can have over 1 million transistors in an integrated-circuit package that is roughly 1 inch square. Microprocessors are at the heart of all personal computers. When memory and power are added to a microprocessor, all the pieces, excluding peripherals, required for a computer are present. The most popular lines of microprocessors today are the 680x0 family from Motorola, which powers the Apple Macintosh line, and the 80x86 family from Intel, which is at the core of all IBM PC–compatible and PS/2 computers. *See also* 6502, 65816, 6800, 68000, 68020, 68030, 68040, 80286, 80386DX, 80386SX, 8080, 8086, 8088, 88000, DECchip 21064, i486DX, i486DX2, i486SL, i486SX, Pentium, Pentium Pro, PowerPC, SPARC, Z80.

microprogramming \mī`krō-prō´gram-ēng\ *n.* The writing of microcode for a processor. Some systems, chiefly minicomputers and mainframes,

change, so as to keep the phosphors irradiated. **2.** To recharge dynamic random access memory chips (DRAMs) so that they continue to retain the information stored in them. Circuitry on the memory board automatically performs this function. *See also* refresh cycle.

refreshable \rə-fresh´ə-bl\ *adj.* In programming, referring to a program module capable of being replaced in memory without affecting processing of the program or the information being used by the program.

refresh cycle \rə-fresh´ sī`kl\ *n.* The process in which controller circuitry provides repeated electric pulses to dynamic random access memory chips in order to renew the stored electric charges in those locations that contain binary 1. Each pulse is one refresh cycle. Without constant refreshing, dynamic semiconductor RAM loses any information stored in it—as it does when the computer is turned off or when the power fails. *See also* dynamic RAM, static RAM.

refresh rate \rə-fresh´ rāt`\ *n.* In reference to video hardware, the frequency with which the entire screen is redrawn to maintain a constant, flicker-free image. On TV screens and raster-scan monitors, the electron beam that lights the phosphor coating on the inner surface of the screen typically refreshes the entire image area at a rate of about 60 hertz, or 60 times per second. (Interlaced monitors, which redraw alternate lines during each sweep of the electron beam, actually refresh any particular line only 30 times per second. Because odd and even lines are refreshed on successive sweeps, however, the effective refresh rate is 60 times per second.)

REGEDIT \rej´ed`it\ *n. See* Registry Editor.

regenerate \rē-jen´ər-āt\ *vb. See* rewrite.

regeneration buffer \rē-jen-ər-ā´shən buf`ər\ *n. See* video buffer.

regenerator \rē-jen´ər-ā`tər\ *n. See* repeater.

region \rē´jən\ *n.* **1.** An area dedicated to or reserved for a particular purpose. **2.** In video programming, a contiguous group of pixels that are treated as a unit. On the Apple Macintosh, for example, a region is an area in a grafPort that can be defined and manipulated as an entity. The visible working area within a window is an example of a region. *See also* grafPort.

region fill \rē´jən fil`\ *n.* In computer graphics, the technique of filling a defined region on the screen with a selected color, pattern, or other attribute. *See also* region.

register \rej´i-stər`\ *n.* A set of bits of high-speed memory within a microprocessor or other electronic device, used to hold data for a particular purpose. Each register in a central processing unit is referred to in assembly language programs by a name such as *AX* (the register that contains the results of arithmetic operations in an Intel 80x86 processor) or *SP* (the register that contains the memory address of the top of the stack in various processors).

registration \rej`ə-strā´shən\ *n.* The process of precisely aligning elements or superimposing layers in a document or a graphic so that everything will print in the correct relative position. *See also* registration marks.

registration marks \rej-ə-strā´shən märks`\ *n.* Marks placed on a page so that in printing, the elements or layers in a document can be arranged correctly with respect to each other. Each element to be assembled contains its own registration marks; when the marks are precisely superimposed, the elements are in the correct position. See the illustration.

Registration marks.

Registry or **registry** \rej´is-trē`\ *n.* A central hierarchical database in Windows 95 and Windows NT used to store information necessary to configure the system for one or more users, applications, and hardware devices. The Registry contains information that Windows 95 and Windows NT continually reference during operation, such as profiles for each user, the applications installed on the computer and the types of documents each can create, property sheet settings for folders and application icons, what hardware exists on the system, and which ports are being used. The Registry

EXHIBIT 28

IEEE Std 100-1992

The New IEEE Standard Dictionary of Electrical and Electronics Terms

[Including Abstracts of All Current IEEE Standards]

Fifth Edition

Gediminas P. Kurpis, Chair

Christopher J. Booth, Editor

The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

ISBN 1-55937-240-0

January 15, 1993

SH15594

selection sort; propagation sort; sifting sort. *Contrast with:* **cocktail shaker sort.** 610.5-1990

Buchmann-Meyer pattern (mechanical recording). *See:* **light pattern.**

buck arm. A crossarm placed approximately at right angles to the line crossarm and used for supporting branch or lateral conductors or turning large angles in line conductors. *See:* **tower.** [10]

bucket (1) (power line maintenance). A device designed to be attached to the boom tip of a line truck, crane, or aerial lift and support workers in an elevated working position. It is normally constructed of fiberglass to reduce its physical weight, maintain strength, and obtain good dielectric characteristics. *Syn:* **basket.** 516-1987

(2) (data management). (A) An area of storage that may contain more than one record and that is referenced as a whole by some addressing technique. (B) In hashing, a section of a hash table that can hold all records with identical hash values. 610.5-1990

(3) (power-line maintenance). A device designed to be attached to the boom tip of a line truck, crane, or aerial lift and support workers in an elevated working position. It is normally constructed of fiberglass to reduce its physical weight, maintain strength, and obtain good dielectric characteristics. *Syn:* **basket.** 516-1987

buffalo. *See:* **conductor grip.** 516-1987

buffer (1) (buffer storage) (supervisory control, data acquisition, and automatic control). (A) A device in which data are stored temporarily, in the course of transmission from one point to another; used to compensate for a difference in the flow of data, or time of occurrence of events, when transmitting data from one device to another. (B) An isolating circuit used to prevent a driven circuit from influencing a driving circuit. C37.1-1987

(2) (data processing and computation). A storage device used to compensate for a difference in rate of flow of information or time of occurrence of events when transmitting information from one device to another. 162-1963

(3) (elevator design). A device designed to stop a descending car or counterweight beyond its normal limit of travel by storing or by absorbing and dissipating the kinetic energy of the car or counterweight. *See:* **elevator.** [119]

(4) (relay). *See:* **relay spring stud.**

(5) (computers). (A) A device or storage area used to store data temporarily to compensate for differences in rates of data flow, time of occurrence of events, or amounts of data that can be handled by the devices or processes involved in the transfer or use of the data. *Syn:* **input buffer; input/output area; output buffer.** (B) A routine that accomplishes the objectives in (A). (C) To allocate, schedule, or use devices or storage areas as in (A). *See also:* **anticipatory buffering; dynamic buffering; simple buffering.** 610.5-1990, 610.12-1990

buffer amplifier (1) (general). An amplifier in which the reaction of output-load-impedance variation on the input circuit is reduced to a minimum for isolation purposes. *See:* **amplifier.** 145-1983

(2) (analog computers). An amplifier in which the reaction of the output-load-impedance variation on the input circuit is reduced to a constant for isolation purposes on the input circuit. *See:* **unloading amplifier.** 165-1977

buffered input. Input that is received using buffers. 610.5-1990

buffered interconnect (BI) (FASTBUS acquisition and control). A device that implements an intersegment connection such that the FASTBUS protocol (FBP) on one segment is not synchronized with that on the other. 960-1986

buffer memory (sequential events recording systems). The memory used to compensate for the difference in rate of flow of information or time of occurrence of events when transmitting information from one device to another. *See:* **buffer; event; storage.** [1]

buffer pool. A collection of buffers that can be allocated and used as needed. 610.5-1990

buffers (buffer salts). Salts or other compounds that reduce the changes in the pH of a solution upon the addition of an acid or alkali. *See:* **ion.** [119]

buffer salts. *See:* **buffers.**

buffer storage (1). An intermediate storage medium between data input and active storage. [61]

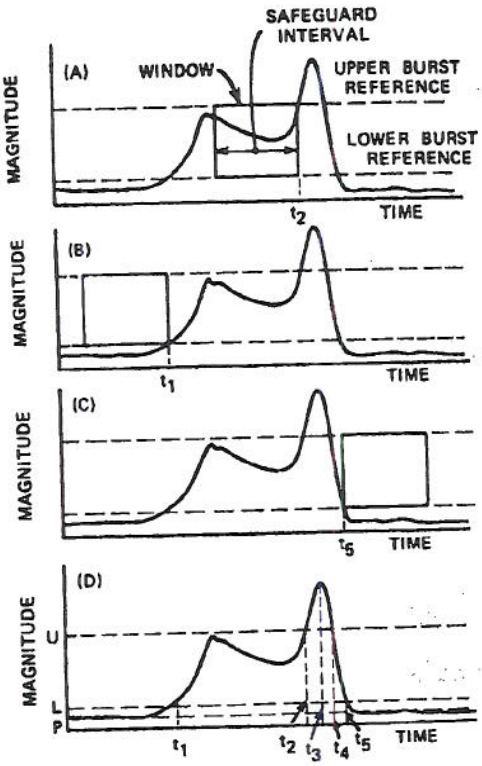
(2) (data management). A storage device that is used as a buffer. *Syn:* **buffer store.** 610.5-1990

(3) (telecommunications). Memory provided in a digital switching system or digital facility interface (DFI) to compensate for timing drift and frame registration differences between a DFI and the switching system. Reduces the probability of slips caused by environmentally produced phase modulation, such as those resulting from diurnal temperature variations. The mechanism for absorbing slips in the DFI of a local digital switch could consist of several single frame stores that are alternately written and read. This scheme allows the two clocks to drift within the limits of the buffer storage. In addition, a type of hysteresis should be provided at the DFI whereby a buffer that was involved in a slip is protected against an immediate slip in the reverse direction. Enough buffering should be used to minimize such occurrences. 973-1990

buffer store. *See:* **buffer storage.** 610.5-1990

buffing (electroplating). The smoothing of a metal surface by means of flexible wheels, to

The right-hand side of the window marks the burst leading-edge time. (C) The burst trailing edge time is found by a similar procedure. The window is slid to the right past its position in (A) until the trace disappears from the window. The left-hand side of the window marks the burst trailing-edge time. (D) Terms used in defining a burst: burst leading-edge time, t_1; burst build-up interval, $t_2 - t_1$; burst rise interval, $t_3 - t_1$; burst trailing-edge time, t_5; burst decay interval, $t_5 - t_3$; burst fall-off interval, $t_5 - t_4$; burst duration, $t_5 - t_1$; upper burst reference, U; lower burst reference, L; long-time average power, P. *See:* **burst.** 257-1964w, [32]



Plot of instantaneous magnitude versus time to illustrate terms used in defining a burst.

Burst Duration

burst duty factor (audio and electroacoustics). The ratio of the average burst duration to the average spacing. *Note:* This is equivalent to the product of the average burst duration and the burst repetition rate. *See:* **burst.** 257-1964w, [32]

burst fall-off interval (audio and electroacoustics). The time interval between the instant at which the upper burst reference is last equaled and the burst trailing edge time. *See:* **burst.** 257-1964w, [32]

burst flag (television). A keying or gating signal used in forming the color burst from a chrominance subcarrier source. *See:* **television.** [34]

burst gate (television). A keying or gating device or signal used to extract the color burst from a color picture signal. *See:* **television.** [34]

burst keying signal (television). *See:* **burst flag; television.**

burst leading-edge time (audio and electroacoustics). The instant at which the instantaneous burst magnitude first equals the lower burst reference. *See:* **burst (audio and electroacoustics).** 257-1964w, [32]

burst magnitude, instantaneous. *See:* **instantaneous burst magnitude.**

burst measurements. *See:* **energy density spectrum.**

burst-quiet interval (audio and electroacoustics). The time interval between successive bursts during which the instantaneous magnitude does not equal the upper burst reference. *See:* **burst (audio and electroacoustics).** 257-1964w, [32]

burst repetition rate (audio and electroacoustics). The average number of bursts per unit of time. *See:* **burst (audio and electroacoustics).** 257-1964w, [32]

burst rise interval (audio and electroacoustics). The time interval between the burst leading-edge time and the instant at which the peak burst magnitude occurs. *See:* **burst (audio and electroacoustics).** 257-1964w, [32]

burst safeguard interval (audio and electroacoustics). A time interval of selected length during which excursions below the lower burst reference are neglected; it is used in determining those instants at which the lower burst references are first and last equaled during a burst. *See:* **burst (audio and electroacoustics).** 257-1964w, [32]

burst spacing (audio and electroacoustics). The time interval between the burst leading-edge times of two consecutive bursts. *See:* **burst (audio and electroacoustics).** 257-1964w, [32]

burst trailing-edge time (audio and electroacoustics). The instant at which the instantaneous burst magnitude last equals the lower burst reference. *See:* **burst (audio and electroacoustics).** 257-1964w, [32]

burst train (audio and electroacoustics). A succession of similar bursts having comparable adjacent burst-quiet intervals. *See:* **burst (audio and electroacoustics).** 257-1964w, [32]

bus (1) (power switchgear). A three-phase junction common to two or more ways. C37.71-1984

(2) (signals and paths) (microcomputer system bus). A signal line or a set of lines used by

an interface system to connect a number of devices and to transfer information. 796-1983
(3) (signals and paths) (696 interface devices). A set of signal lines used by an interface system, to which a number of devices are connected, and over which information is transferred between the devices. 696-1983
(4) (power switchgear). A conductor, or group of conductors, that serve as a common connection for two or more circuits. C37.100-1981
(5) (programmable instrumentation). A signal line or set of signal lines used by an interface system to which a number of devices are connected and over which messages are carried. 488.1-1987
(6) (electronic computers). One or more conductors used for transmitting signals or power from one or more sources to one or more destinations. 162-1963
(7) (SBX bus). A signal line or set of signal lines used by an interface system to connect a number of devices and to transfer data. 959-1987
(8) (STEbus). A signal line or set of lines used by an interface system to connect a number of devices, and over which information is conveyed. 1000-1987
(9) (simple 32-bit backplane bus). A set of signal lines to which a number of devices are connected and over which information is transferred between them. 1196-1987
(10) (hydroelectric power plants). A conductor or group of electrical conductors serving as common connections between circuits, generally in the form of insulated cable, rigid rectangular or round bars, or stranded overhead cables held under tension. 1020-1988
(11) (metropolitan area networks). The concatenation of the transmission links between nodes and the data path within nodes that provides unidirectional transport of the digital bit stream from the head of bus function past the access unit (AU) of each node to the end of bus. *Note:* This differs from the bidirectional bus as used in ISO/IEC 8802-3:1990 [IEEE Std 802.3-1990] and ISO/IEC 8802-4:1990 [IEEE Std 802.4-1990]. 802.6-1990

bus clock cycle. An amount of time equal to one bus clock period, nominally 100 ns. 1296-1987

bus cycle (1) (general system terms) (microcomputer system bus). The process whereby digital signals effect the transfer of data bytes or words across the interface by means of an interlocked sequence of control signals. Interlocked denotes a fixed sequence of events in which one event must occur before the next event can occur. 796-1983
(2) (signals and paths) (696 interface devices). The basic sequence of electrical events required to complete a transfer of data on the bus. A bus cycle contains at least three bus states. 696-1983

bushing (1) (power switchgear). An insulating structure including a through conductor, or providing a passageway for such a conductor, with provision for mounting on a barrier, conducting or otherwise, for the purpose of insulating the conductor from the barrier and conducting current from one side of the barrier to the other. C37.100-1981
(2) (power and distribution transformer). An insulating structure including a central conductor, or providing a central passage for a conductor, with provision for mounting on a barrier, conducting or otherwise, for the purpose of insulating the conductor from the barrier and conducting current from one side of the barrier to the other. C57.12.80-1978
(3) (rotating machinery) (electrical). Insulator to permit passage of a lead through a frame or housing. [9]
(4) (relay). *See:* **relay spring stud.**

bushing insert (separable insulated connectors). A connector component intended for insertion into a bushing well. 386-1985

bushing potential tap (outdoor apparatus bushings). An insulated connection to one of the conducting layers of a bushing providing a capacitance voltage divider to indicate the voltage applied to the bushing. 21-1976

bushing, rotor. *See:* **rotor bushing.**

bushing tap (partial discharge measurement in liquid-filled power transformers and shunt reactors). Connection to a capacitor foil in a capacitively graded bushing designed for voltage or power factor measurement that also provides a convenient connecting point for partial discharge measurement. The tap-to-phase capacitance is generally designated as C_1 and the tap-to-ground capacitance is designated as C_2. *See:* **bushing potential tap; bushing test tap; capacitance (of bushing).** [125]
(2). Connection to a capacitor foil in a capacitively graded bushing designed for voltage or power factor measurement that also provides a convenient connecting point for partial discharge measurement. The tap-to-phase capacitance is generally designated as C_1, and the tap-to-ground capacitance is designated as C_2. *See:* **bushing potential tap, bushing test tap, capacitance (of bushing)** in IEEE Std 21-1976. C57.113-1988

bushing test tap (outdoor apparatus bushings). An insulated connection to one of the conduction layers of a bushing for the purpose of making insulation power factor tests. 21-1976

bushing-type current transformer (power and distribution transformer). One that has an annular core and a secondary winding insulated from and permanently assembled on the core but has no primary winding or insulation for a primary winding. This type of current transformer is for use with a fully insulated conductor as the primary winding. A bushing-type current transformer usually is used in equip-

CERTIFICATE OF SERVICE

I hereby certify that on November 6, 2007, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF which will send electronic notification of such filing to the following:

John G. Day, Esquire
Steven J. Balick, Esquire
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Additionally, I hereby certify that true and correct copies of the foregoing were caused to be served on November 6, 2007 upon the following individuals in the manner indicated:

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